Interdependent Interference in Multi-Core Architectures

DESCRIPTION

Software of (hard) real-time systems have to undergo rigorous verification of correctness, which includes verification whether the software meets all deadlines. An important aspect of this verification is timing analysis, which aims at determining a tight bound on the total execution time of a real-time computation (aka. task). A major challenge for timing analysis in multi-core systems is to determine the interference on the task's execution time by software running on other cores in parallel. This interference might be caused by shared resources, such as shared caches or shared buses, between the cores and may considerably increase the total execution time of a task.

Another important phenomenon that may complicate this analysis are timing anomalies. These are situations where a locally favorable event during the execution of real-time software eventually leads to a global increase of the execution time. A typical example of such a situation is a cache hit (i.e., a hit is locally favorable compared to a miss since it takes less time) that impacts the way in which instructions are executed in an out-of-order processor pipeline (i.e., instructions are executed sequentially due to data dependencies instead of parallel). Both, multi-core interference and timing anomalies, may lead to state space explosion and may render the determination of safe execution time bounds practically impossible.

The objective of this post-doc position is to investigate the relationship between a) different sources of interference in multi-core architectures as well as b) multi-core interference and timing anomalies. In the later case we are interested in studying how to characterize interactions between different forms of interference. For instance, two memory requests originating from two different cores may interfere at the level of shared caches, shared buses, and eventually the shared memory. Naturally the interference at higher levels of the memory hierarchy may impose a (partial) ordering of memory requests. The objective his thus to study possible cancellation effects, but also possible amplification effects. Such amplification effects may, in fact, resemble timing anomalies and thus make it impossible to analyze the two sources of interference independently from each other.

The considered phenomena will be studied either directly by tracing executions on a suitable hardware platform or using abstract modeling/simulation (e.g. via model checking). Different scenarios of interdependent interference should be exposed and analyzed w.r.t their root causes in order to facilitate finding similar situations, e.g. on other hardware platforms. If time permits adapted analysis techniques that either take inter-dependencies into account should be developed or analysis techniques to (formally) analyze the characteristics of a hardware platform in order to rule out/detect such phenomena.

REQUIREMENTS/SKILLS

Candidates need a PhD (or equivalent) preferably in a domain related to the topic (interference, timing analysis, real-time systems). In addition profound knowledge of computer architecture design (processor cores, memory hierarchy) are required. A background in static program analysis (abstract interpretation, symbolic execution, ...).
and formal methods (e.g., model checking) is important.

**ADMINISTRATIVE DETAILS**

The position is to be filled by fall 2023. The successful candidate will work for the ANR project CAOTIC at Télécom Paris (Palaiseau, France) within the ACES team. The net salary ranges between 2300 and 2500 EUR.

**REFERENCES**


*Speculative Execution and Timing Predictability in an Open Source RISC-V Core.* Alban Gruin, Thomas Carle, Hugues Cassé, Christine Rochange: RTSS 2021 *DOI*


*Scaling Up the Memory Interference Analysis for Hard Real-Time Many-Core Systems.* Maximilien Dupont de Dinechin, Matheus Schuh, Matthieu Moy, Claire Maiza: DATE 2020 *DOI*

**APPLICATION**

Interested candidates may apply [online](#).

**CONTACT**

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