Joint IEEE & SoC^2 Day

On

Inversion Coefficient & RF Low Power

October the 12th of 2021

CIME Nanotech, 3 parvis Louis Néel, GRENOBLE.

Context:

The development of advanced technologies is changing the way RF circuits are designed. In the 90s, the growing interest for telecommunications and GSM pushed designers to use CMOS technologies in order to reduce fabrication costs which were an issue to address mass markets. At this time, the low FT of available technologies has pushed designers to work in high inversion in order to meet the requirements in terms of bandwidth. Many design methods have emerged based on the small signal model of the transistor in strong inversion region of operation.

Today, the paradigm is changing. Advanced technologies have very high FT and the demand for low power systems is very high. The issue of mobility or Internet of Things appeal for a break in the consumption of RF circuits. The use of the MOS in strong inversion is no longer necessary and the trend is moving towards polarization in low or moderate inversion regime. Indeed, the efficiency of the component in terms of energy, characterized by the inversion coefficient or the g_m / Id ratio, increases when the channel inversion decreases.

In addition, the analytical models of the MOS based on the different operating regions are no more useful for designer when advanced technologies are considered. This leads to an intensive use of tuning operations in RFIC design which reduces the link between technology and design.

The aim of this IEEE – SoC2 joint day is to present new RF design technics dedicated to low power applications. Morning keynotes will focus on inversion coefficient based design technics for RF low power. Afternoon presentation will be extended to other low power design technics in order to have a larger scope on recent advances in RF low power application.

Preliminary Program:

9:00 - Welcome Coffee

9:30 - Morning Keynote 1 : Inversion coefficient based MOS model

Abstract:
Compact MOSFET models are indispensable tools for both circuit design and simulation. Many of the existing MOSFET models, however, are not appropriate for design due to reasons such as lack of accuracy, complex equations to describe the MOSFET behavior, excessive number of parameters, and lack of physical meaning of parameters. The ACM model is the result of a fresh look at the problem of MOSFET compact modeling. It marries a physics-based approach with former semi-empirical models. ACM adopted the charge-based approach pioneered by Maher and Mead in 1987 and the unified charge control model (UCCM), presented by Byun et al. in 1990. Since the MOS transistor is the basic component of modern electronics, a careful presentation of its basic theory will be given. Instead of the usual approach of furnishing separate analytical formulas for the strong and weak inversion regions of the MOS transistor, we provide simple formulas which are valid in all operating regions, including moderate inversion. This unified design approach, which is particularly suitable for the design in advanced CMOS technologies, allows the insightful exploration of the design space.

Speaker : Carlos Galup-Montoro
Carlos Galup-Montoro (M'89) studied Engineering Sciences at the University of the Republic, Montevideo, Uruguay, and Electronic Engineering at the National Polytechnic School of Grenoble (INPG), France. He received an Engineering degree in electronics in 1979 and a doctorate degree in 1982, both from INPG. From 1982 to 1989 he worked at the University of São Paulo, Brazil. Since 1990 he has been with the Electrical Engineering Department, Federal University of Santa Catarina, Florianópolis, Brazil, where he is now a Professor. From August 1997 to February 1998 he was a Research Associate with the Analog Mixed Signal Group, Texas A&M University. From August 2008 to July 2009 he was a Visiting Scholar at the University of California, Berkeley

10:30 – Coffee Break

11:00 - Morning Keynote 2 : RF Circuit Design with the Inversion Coefficient, *application to LNA implementations*

Abstract: The emergence of the Internet of Things (IoT) poses stringent requirements on the energy consumption and has hence become the primary driver for low-power analog and RF circuit design. Implementation of increasingly complex functions under highly constrained power

and area budgets, while circumventing the challenges posed by modern device technologies, makes analog and RF circuit design ever more challenging. Some guidance would therefore be invaluable for the designer to navigate the multi-variable design space.
This talk is related to the design of RF CMOS building blocks involving technology considerations, circuit techniques and synthesis. First a brief on the inversion coefficient (IC) basics and the analog/RF figure of merit is proposed. Then a 3-step design methodology based on the IC is detailed. Integrated in a design interface the methodology is further exploited to develop RF Low Noise Amplifiers (LNA). Two applications are considered to illustrate it: Wide Band Inductorless LNA for multi-mode/multi-standard Radio applications, and Ultra Low Power LNA dedicated to 2.4GHz Wireless Sensor Networks. Four LNA topologies designed in three technology nodes (130nm, 65nm and 28nm) are compared and discussed.

Speaker: Thierry TARIS
Thierry TARIS received his Master and PhD degrees from the University of Bordeaux (UB), France, in 2000 and 2003 respectively. He joined the IMS Lab in 2005 as an Associate Professor of UB, and then the Bordeaux Institute of Technology (Bx-INP) in 2014 as a full Professor. His research interests are related to the Radio-Frequency Integrated Circuits in Silicon technologies. More specifically it concerns the design of Low Noise Amplifiers and Mixers, the development of wake-up radio and RF energy harvesters.
Since 2008 he has been enrolled as a coordinator and/or scientific contributor for more than 14 European (MEDEA+, ENIAC program) projects and National (ANR RNRT, FUI, CIFRE, Région Aquitaine) projects. He has published more than 100 papers in international journals and conferences, 3 Best Paper Awards and is co-inventor of 6 patents.
Prof. Taris has led the circuit design group from 2011 to 2014. He was an invited Professor of the University of British Columbia (UBC), Vancouver, Canada, in 2012 and 2014, and Ecole Polytechnic Federal de Lausanne (EPFL), Lausanne, Switzerland, in 2016. For 6 years Dr. Taris has been a board member of the ST-IMS joined lab between the IMS lab and ST-Microelectronics. From 2016 he is an expert for the Strategic Business Area (SBA) of Aerospace Valley.

12:00 – Lunch

13:30 - Afternoon Sessions: RF Low Power Circuits & Design

13:30 – N-Path & WSN (Chairman F. Podevin)

- 13:40 “Introduction to N-Path” – **L. Lançon (IMS)**
- 14:00 “New Architectures for harmonic rejection N-Path mixer” – **S. Ibrahim (RFIC-lab)**
- 14:20 “UWB transmitter for WSN” – **Felipe Artemio (IM2NP/UFPR/RFIC-Lab)**
- 14:40 "Apprentissage et supervision dans les systèmes embarqués ultra-low power"– **S. Marzeti (IM2NP)**

15:00 – Coffee Break

15:20 - Spintronic for RF low power application (Charman Ursula Ebels)

- 15:30 “Spintronic magnetic tunnel junctions for wireless sensor network applications” **I. Bendjeddou (CEA/RFIC-Lab/Gipsa/Spintec)**
- 15 :50 “Vortex spin torque oscillators” **M. Jotta Garcia (Thales/CNRS)**
- 16 :10 “RF-to-DC conversion properties of perpendicular magnetic tunnel junctions operating in the 2-10GHz range and their applications” **A. Sidi El Valli (Spintec)**

16:30 - Gm/Id and IC design technics (Chairman Manuel Barragan)

- 16:40 “Inversion coefficient based model for non-linear design” – **D. Pino Monroy (ST/RFIC-Lab)**
- 17:00 “RF feedback LNA design based on gm/id approach” – **K. Bouchoucha (ST/RFIC-Lab)**
- 17:20 “LNA for quantum application” – **B. Giovani (ST/TIMA)**

17:40 – Closing Coffee

Registration:

Covid-19 issue : Sanitary Pass for french residents or attestation of a complete vaccination process for foreign residents must be sent by email while registering to anne-laure.fourneret@univ-grenoble-alpes.fr.

The workshop participation, including coffee breaks, lunch, etc., is free of any charge. To help the organizers with the logistics please register by sending an e-mail to anne-laure.fourneret@univ-grenoble-alpes.fr at by September the 27th, 2021.