XILINX
UNIVERSITY PROGRAM

Xilinx Adaptive Compute PhD school in association with ETH Zurich XACC: Developing accelerators using FPGAs, 11-15 January 2021

Introduction

Xilinx is the inventor of the FPGA, programmable SoCs, and now, the ACAP. Our highly flexible programmable silicon, enabled by a suite of advanced software and tools, drives rapid innovation across a wide span of industries and technologies.

With the decline of Moore's law, HPC systems need to include specialised heterogeneous accelerators to continue performance scaling. FPGAs are emerging as an ideal target for a range of HPC applications.

XACC PhD School

The XACC PhD school will be hosted virtually by the Xilinx University Program in conjunction with ETH Zurich XACC. The purpose of this school is to offer students an opportunity to learn about FPGA design and recent technology developments, and gain hands-on experience creating FPGA accelerators with Xilinx software.

An introduction to FPGA and Zynq technology will be covered including the PYNQ framework, along with some hands-on tutorials and examples on local hardware (provided by the Xilinx University Program to each attendee). The Xilinx Vitis software development environment for designing FPGA accelerators will be introduced. Vitis supports OpenCL, C and C++. RTL design flows are also supported for experienced hardware developers. Each of these flows will be discussed along with the open-source Xilinx Runtime Library and Vitis open-source accelerated libraries.

Participants will devise and build their own custom accelerators targeting Alveo and AWS F1 instances. Students can follow the guidance of the instructors to build custom designs from available open source libraries or to create their own custom accelerator design.

The school will also include invited presentations from speakers at ETH and Xilinx on relevant topics, including an overview of the XACC program and the XACC at ETH Zurich.

Intended audience

The school is open to international computer science students and related disciplines, and early stage academic researchers. PhD students are especially encouraged to attend.

The school is intended for academics who are new to FPGA and working on compute applications that may benefit from FPGA acceleration.

Pre-requisites

Some basic FPGA awareness would be an advantage, but is not required, although participants should have some knowledge of parallel processing concepts and/or parallel hardware.

Most of the FPGA design work will be carried out in C++. Intermediate C++ programming experience is required.

Xilinx will provide remote access to cloud instances which will be enabled with Xilinx tools and devices. Attendees must have their own laptop with reasonable screen size to effectively use the required software. (Tablet, and Netbook type devices are not suitable.)

Internet connection of suitable quality to attend the video conferencing sessions, participate in discussions, and connect to clouds instances is also required.

Dates and times

09:00 – 18:00 CET daily, 11 – 15 January 2021

This will be a virtual school and will be fully online (Zoom).

Applications

Please apply online by 16 Dec 2020 by completing the following form:

https://www.xilinx.com/support/university/XUP-XACC-School.html

Places are limited. You will receive confirmation of your place shortly after the closing date if your application has been successful. If the school is oversubscribed, a limit on places per institution may be applied.

Contact

Please contact Cathal McCabe (XUP manager EMEA) cathal.mccabe@xilinx.com for any questions related to this school.