PostDoc Position

CMOS Design of Low-Power Wake-Up Receiver for IoT

Opening: The department of Electronics and Communications at Telecom Paris has a postdoc opening for a candidate with an EE background. The candidate is expected to lead the development of a novel wake-up receiver suitable for IoT applications. The key feature of this receiver is its adaptability which allows it to operate at very low power without compromising detectability performance.

Current status and expected work: Over the last few years we have proposed a modular detection algorithm for wake-up receivers and proved its optimality in terms of error rate, delay, and power consumption. This algorithm was then simulated using high level electrical simulations. Results were encouraging as we obtained energy gains of about 50% compared to state-of-the-art solutions. The objective of this project is to push this work to its final state and implement the algorithm at the electrical level using an advanced CMOS process. Collaboration with a leading semiconductor company is expected.

Work description:

1. Study the proposed algorithm.
2. Choose an architecture to implement the algorithm and fine tune its main specifications, e.g., central frequency, sensitivity, message length range.
3. Design and simulate the main blocks of the architecture in an advanced CMOS process.

Required skills:

1. CMOS analog design
2. Signal Processing

Contract Duration: 12 months **Starting date:** Fall 2020

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To apply: Applicants should submit a cover letter, a detailed CV, a research statement (2 pages max.), and provide the names of three references.