Continuous-time Digital Signal Processing for Audio Feature Extraction integrated in 28nm FD-SOI CMOS

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November 8 2017

Outline

I. Context : Voice Activity Detection

II. State-of-the-art

III. Proposed concepts
Opportunities and challenges

Outline

Context

I. Context : Voice Activity Detection

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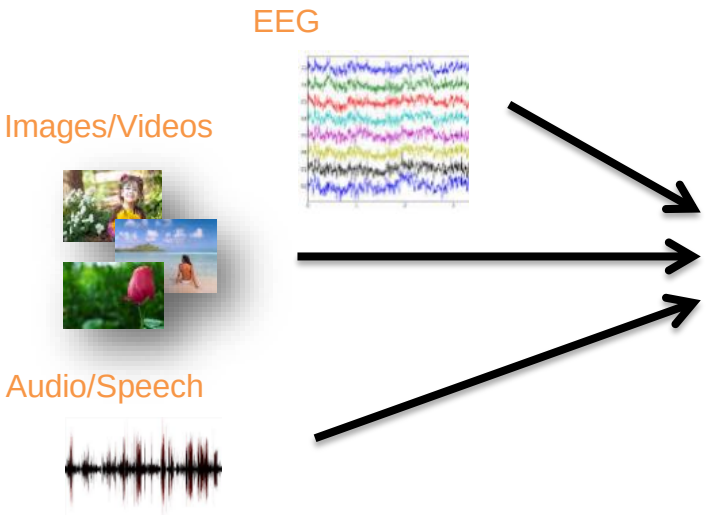
Opportunities and challenges

Ambient Intelligence / IoT

- Massive amounts of data
- Always-on sensing

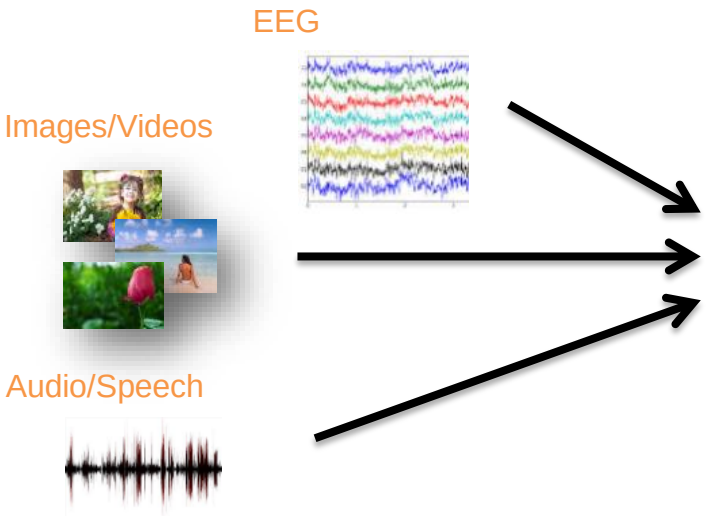


To process locally
OR
to transfer to main computation unit (cloud)

ENERGY HUNGRY

Ambient Intelligence / IoT

- Massive amounts of data
- Always-on sensing



To process locally
OR
to transfer to main computation unit (cloud)

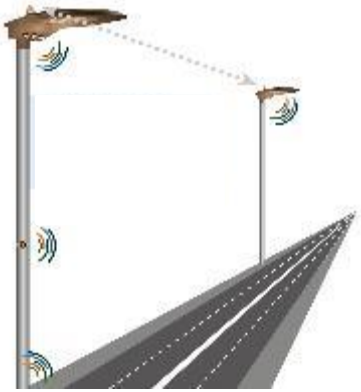
ENERGY HUNGRY

Small, cheap, no battery replacement

→ **Towards Near-Sensor Computing**

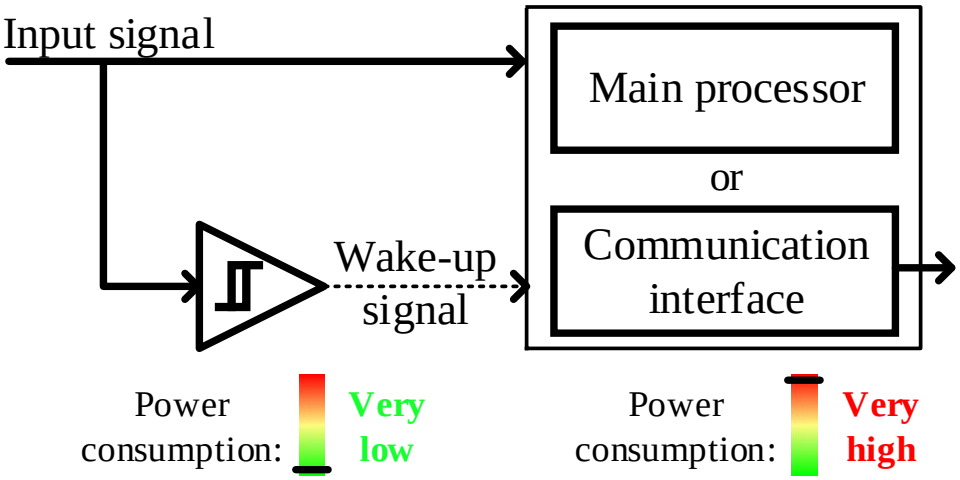
Applications

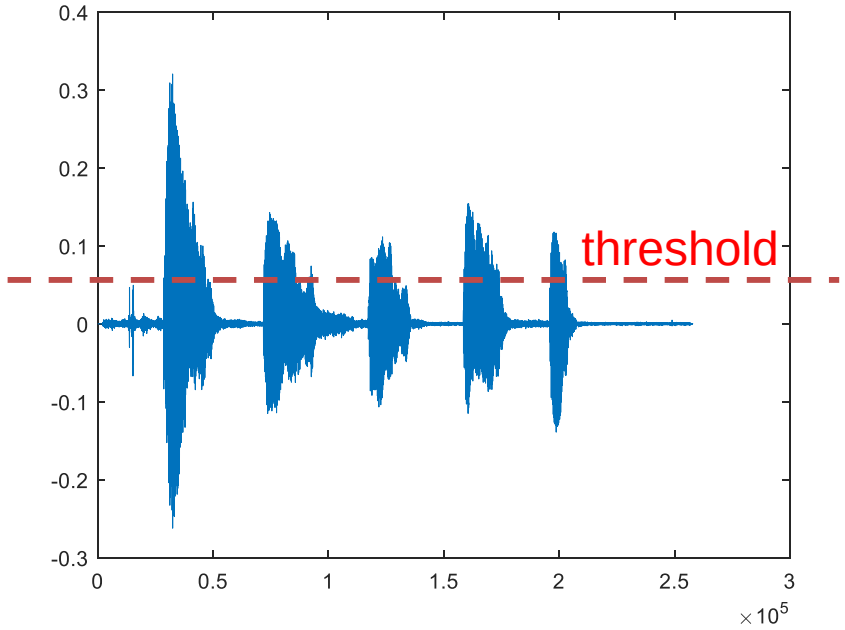
- Audio processing
  - Voice Activity Detection in noisy context
  - Vowels, words, language recognition
  - Specific feature extraction
- Human-body signal classifications
  - ECG, EEG, etc…
- Vibration monitoring
- Image processing
  - Motion-triggered cameras
  - Face detection / Owner-activated devices



Focus on audio processing

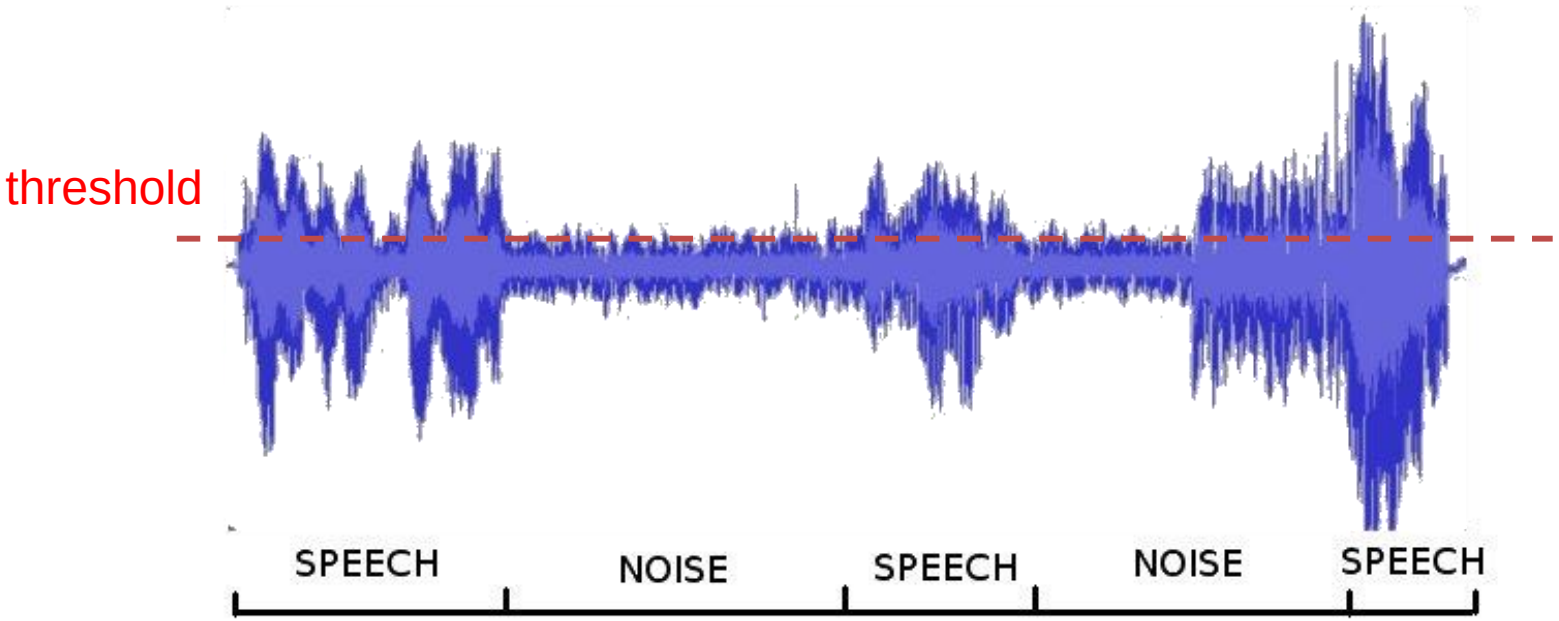
- Example : Voice activity detection





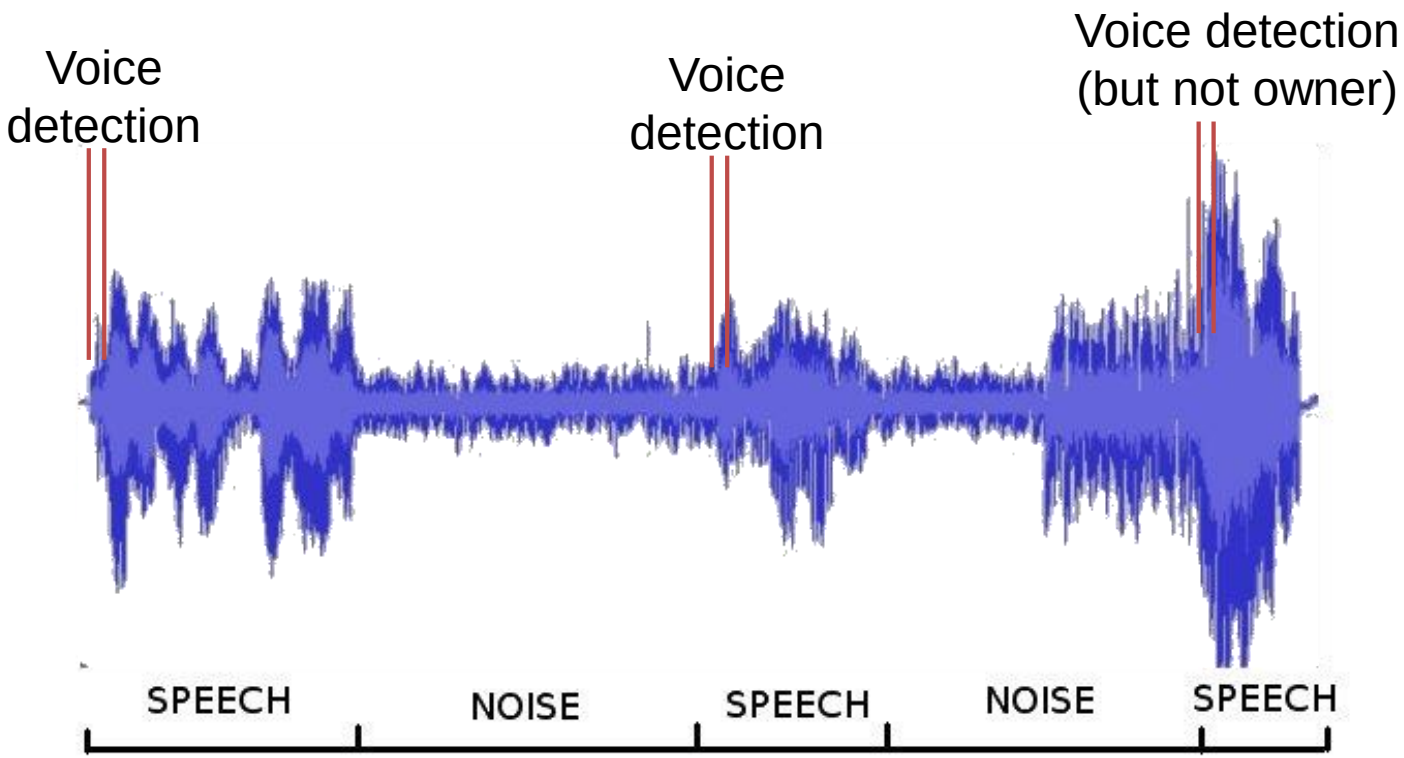
In the presence of noise

- Triggered device is almost always ON !

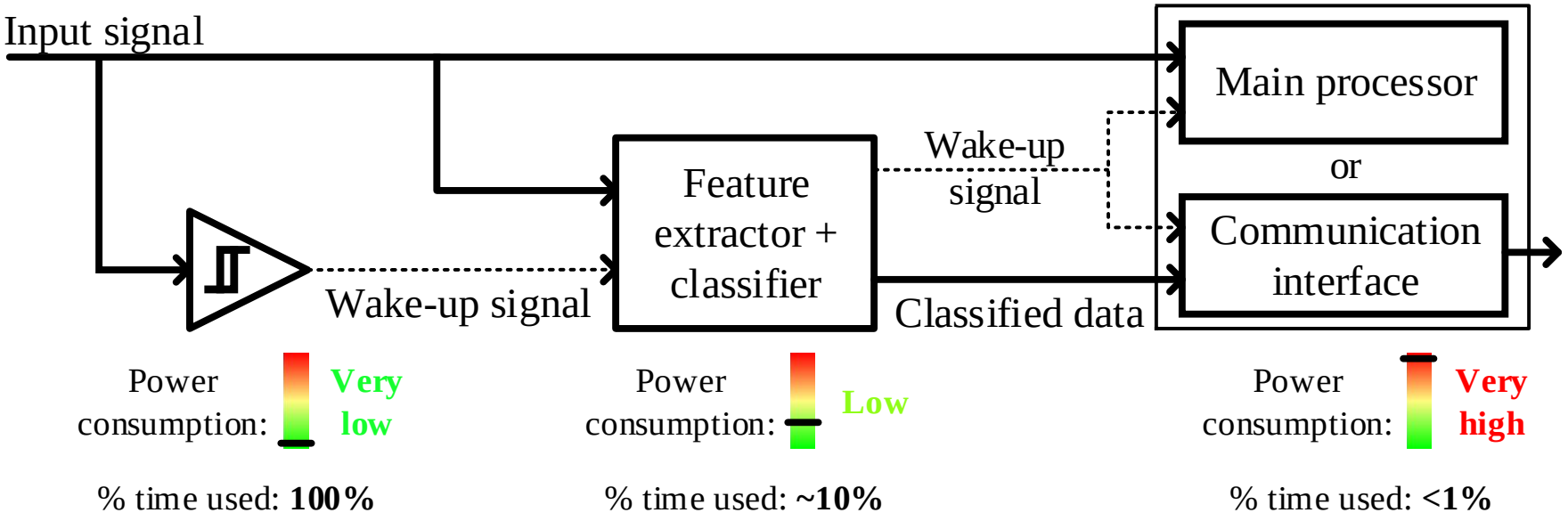


Voice Activity Detection

- « Wake-on-feature »



Embedded processing chain



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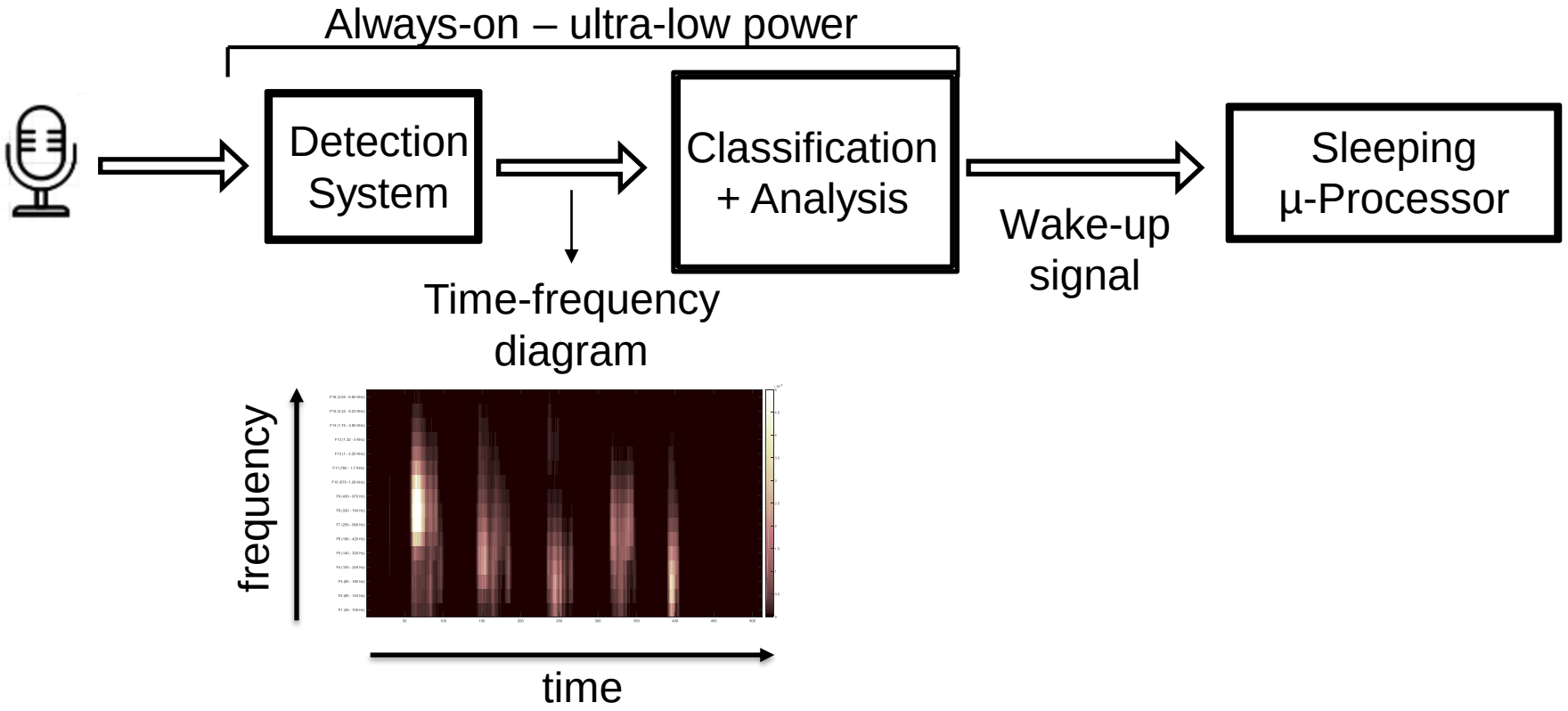
State of the art

VAD State-of-the art

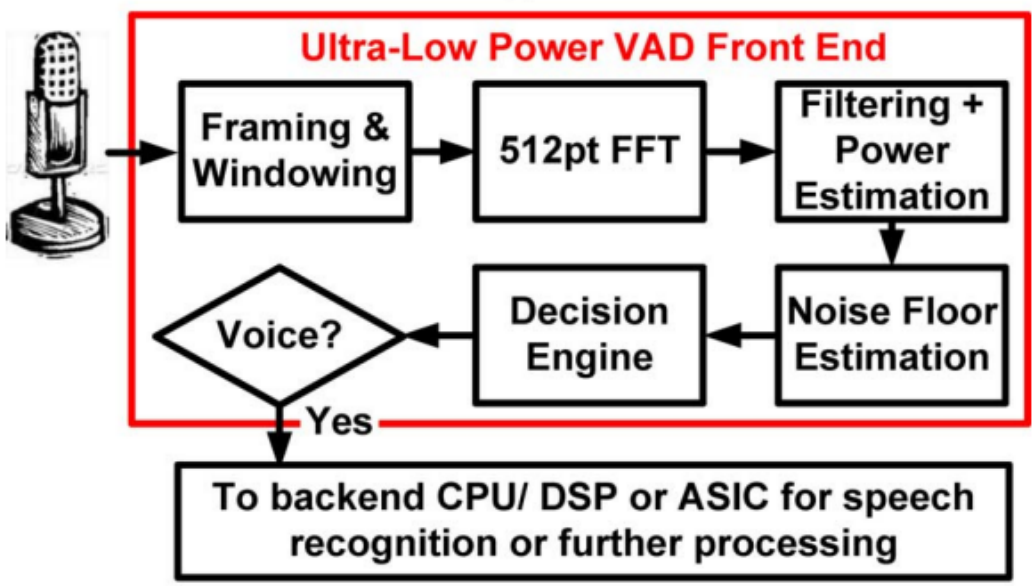


→ Frequency decomposition

Fully digital implementation

[Raychowdhury JSSC Aug 2013]

Georgia Tech / Intel



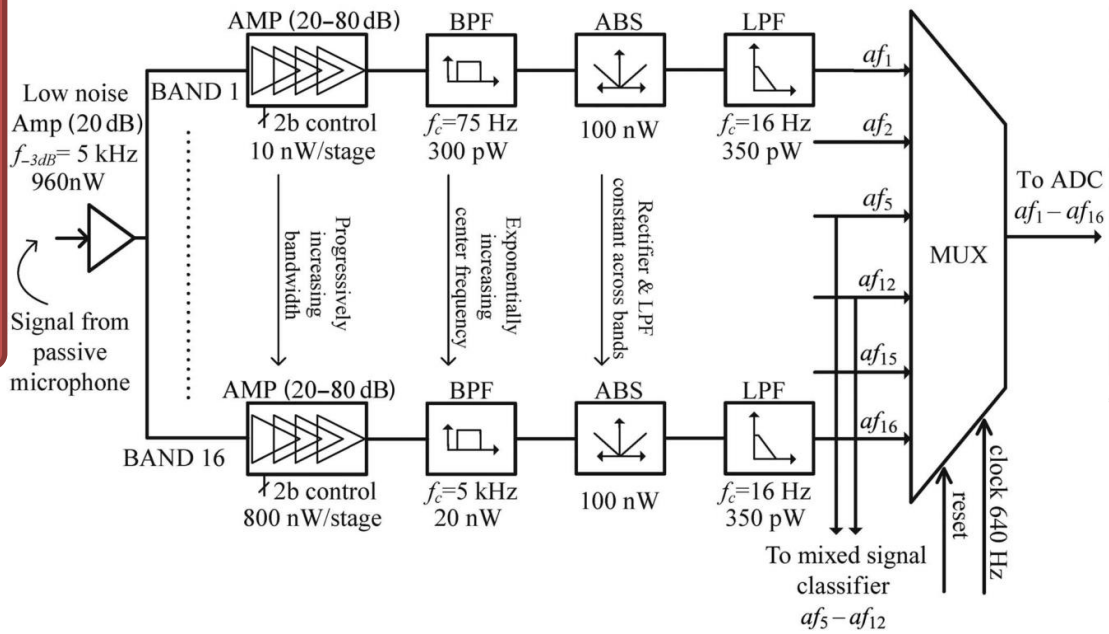
++ **Fully configurable / Highly integrated**

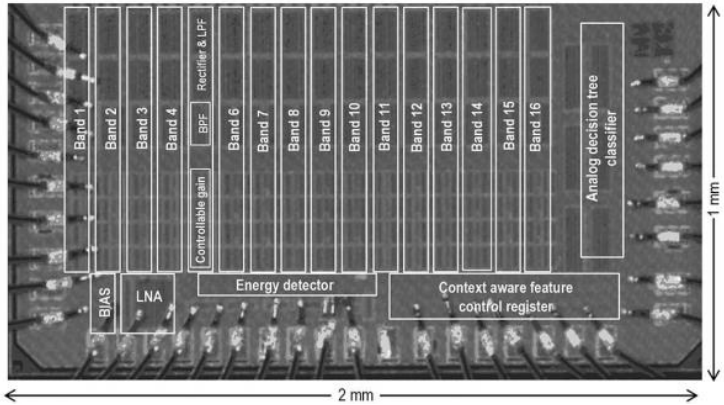
- - **High sample rate (~10MHz) → energy consumption is high**
VAD >100µW (without ADC)

Fully analog implementation

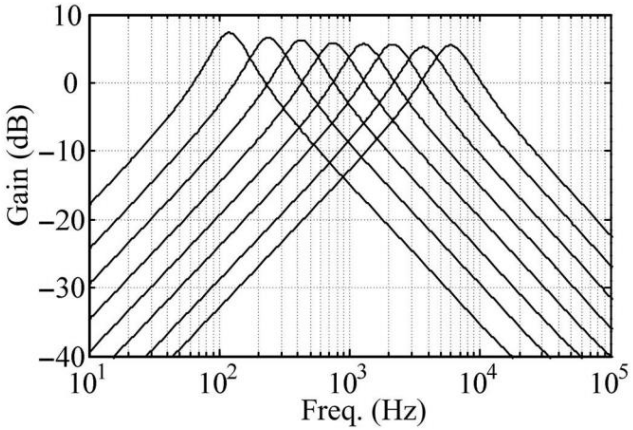
[Badami JSSC Jan 2016]

KU Leuven





90nm chip layout



++ **Power consumtion is low (6µW)**

Simple and efficient classifier

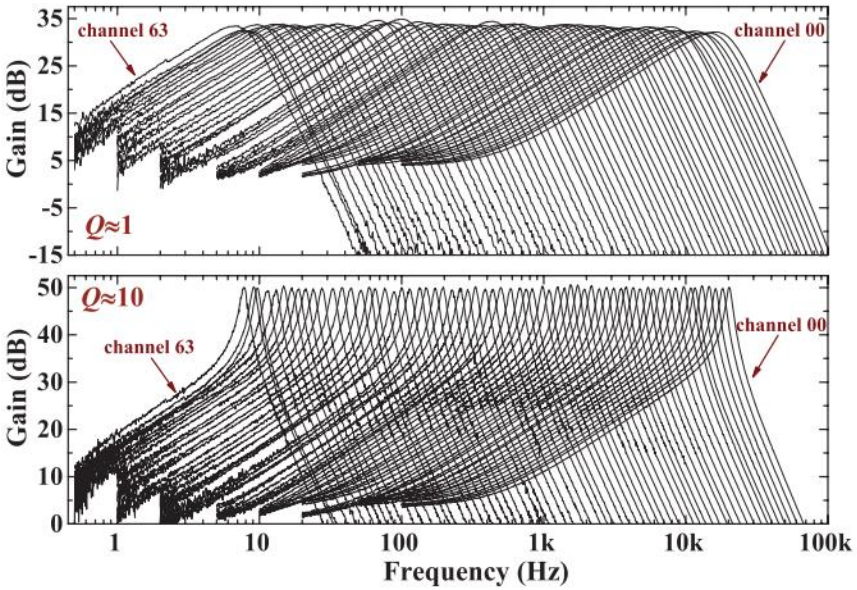
\- - **Large silicon area (2 mm²)**

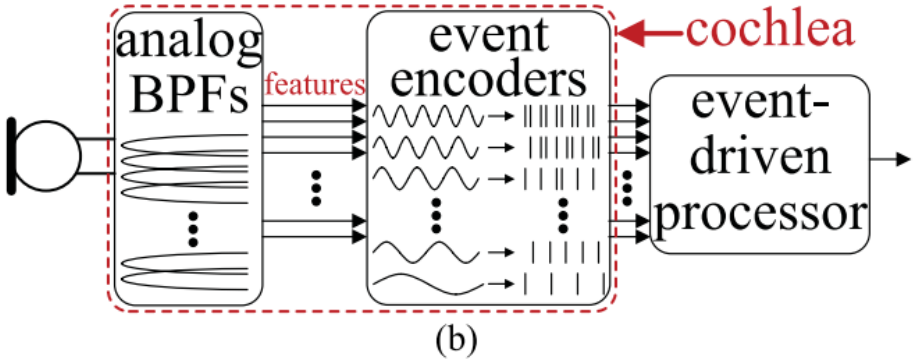
Not flexible / configurable

Analog filter banks + event encoders

[Yang JSSC Nov 2016]

ETH Zurich





0.5 V 55 µW silicon cochlea
64 stereo channels

++ **Enhanced feature resolution**
Bioinspired from human cochlea

- - **Large silicon area (> 50 mm² in 0.18µm CMOS)**

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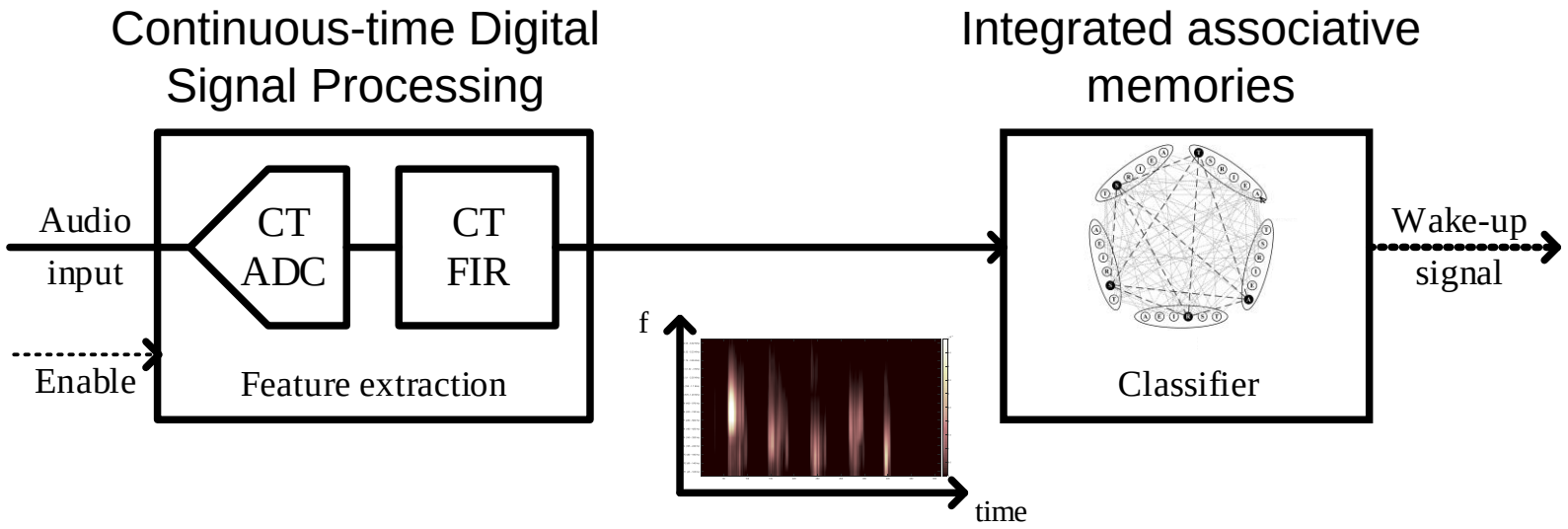
I. Continuous-time DSP

II. Associative memories

Proposed concept

Proposed concept

- Exploring innovative circuit structures in fine-pitch CMOS technologies



Continuous-Time Digital Signal Processing (CTDSP)

Proposed concept

Continuous (CT) ← **Time** → Discrete (DT)

Continuous (CA) ↑ **Amplitude** ↓ Discrete (DA)

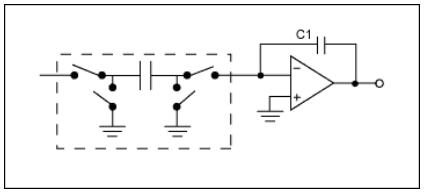
CT CA

Classical analog
Analog filters

DT CA

Sampled analog systems

Ex: Switched-capacitor filters



CT DA

Continuous-Time Digital Signal Processing (CT DSP)

DT DA

Digital Signal Processors
Microprocessors

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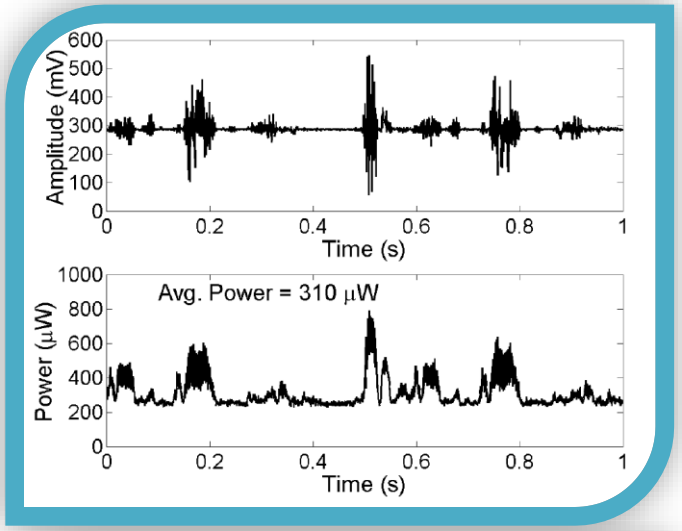
CT DSP Opportunities

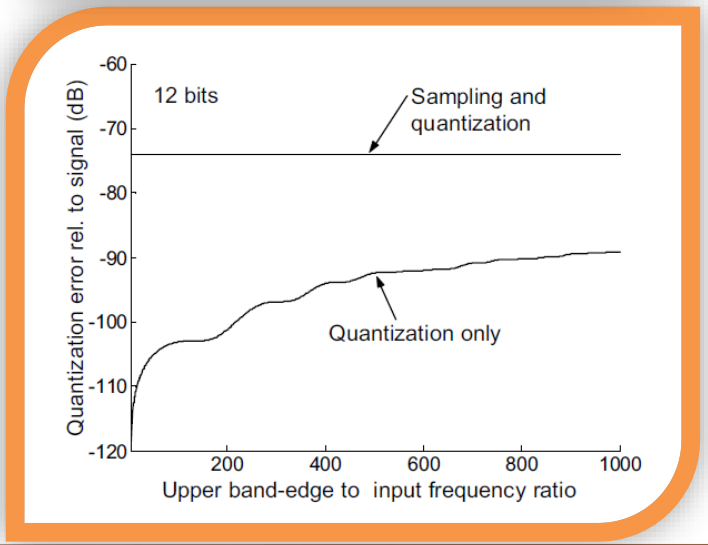
Proposed concept

CMOS Digital System
Configurability
Scalability
High integration level

Event-driven system
No clock
Event-driven power consumption

Quantization-first
No aliasing
Reduced ADC resolution





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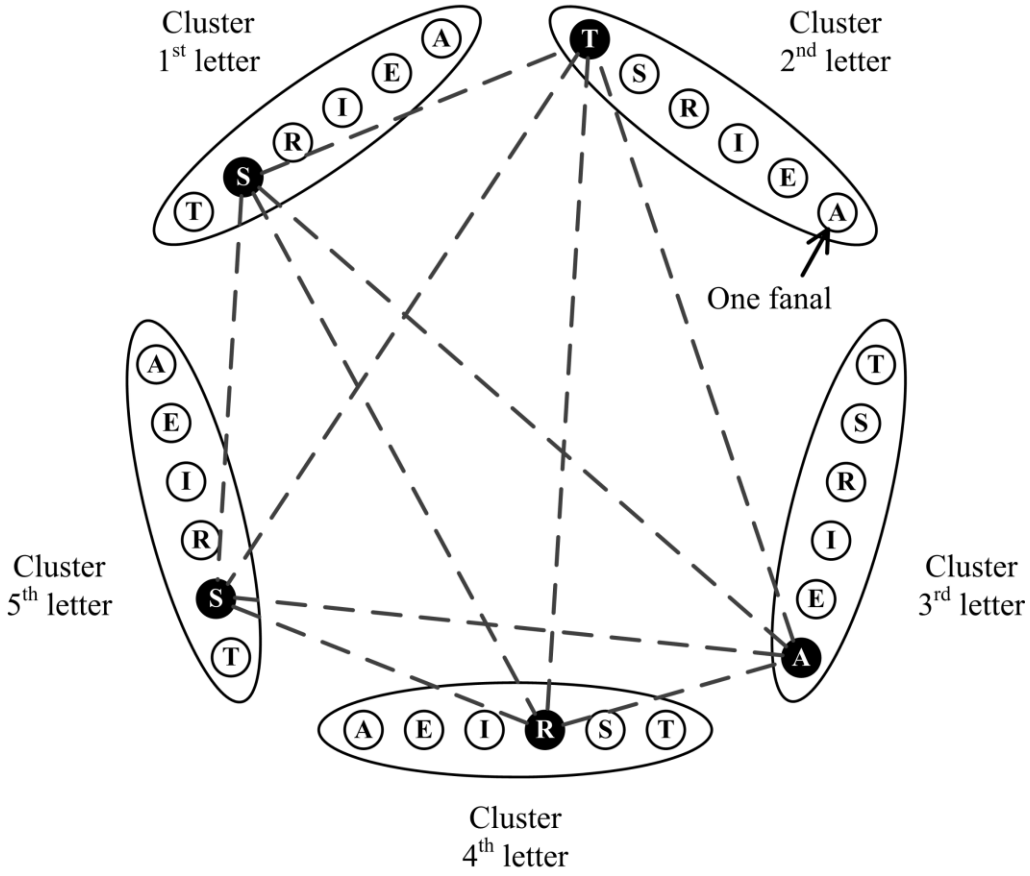
Integrated associative memories

- Example : Clustered clique-based networks

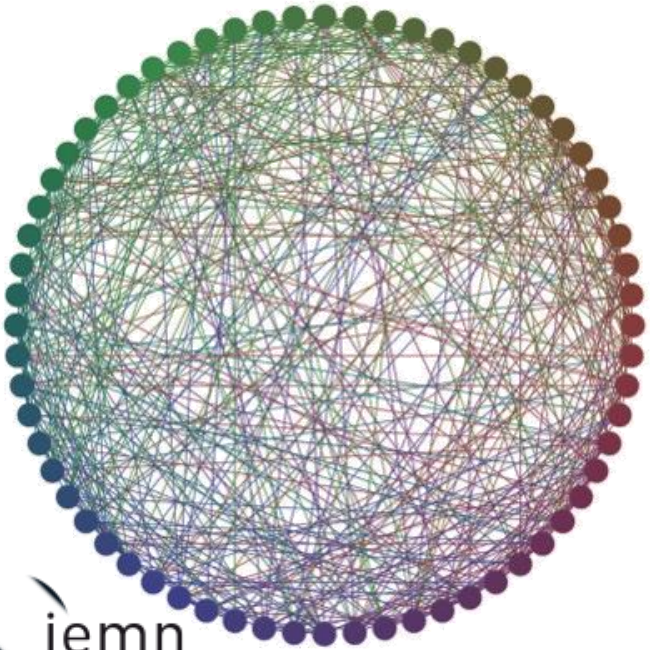


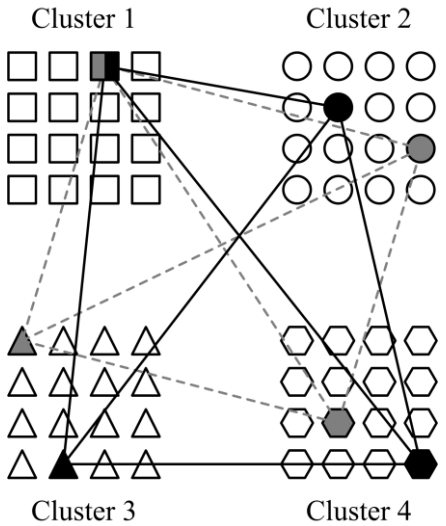
Proposed concept

Integrated associative memories Opportunities

- Suitable for small classification tasks
- Low-energy / application specific
- Robustness

Proposed concept





Small connectivity ratio
(connections / neurons)

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Challenges

Proposed concept

- CT DSP
  - Event-driven processing with no clocks is difficult to handle and design (concepts, tools)
  - Timing is critical…
- Associative memories
  - Generic topology vs. diversity of applications
  - Bridging the gap from theory to efficient hardware
- Latency !
- Integration in advanced CMOS technology

Conclusion

- Proposed radical change in concepts to implement ultra-low power feature extraction and classification
  - Best of both analog and digital worlds
- Demonstration on audio processing
  - CT DSP
  - Associative memories
- Objective : demonstration of a « wake-on feature » highly-efficient embedded system in 28nm FDSOI CMOS

We are open to any suggestions, questions, collaborations, discussions,…

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