THALES
Building a future we can all trust

RISC-V & OpenHW

Thales Research & Technology, France

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Thales Research & Technology France

Key figures

- 240 TRT permanent research staff
- 50+ PhDs
- About 50 pers. Nokia, about 80 pers. CNRS, about 50 pers. GBUs (SIX, DMS, LAS, DIS)
- 50 invention disclosures, 35 patents / year
- 50+ scientific publications / year
- Clean rooms: 4 000 m²
  - 200 characterization & process main equipment
- 1 Nobel Prize, 3 European Research Council projects (ERC)
- 80 French or European on-going collaborative research projects

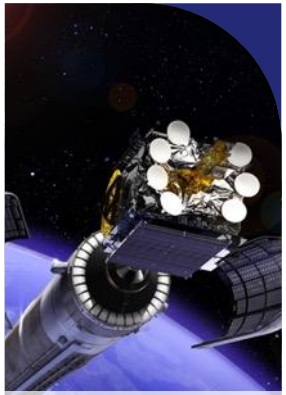
TRT Fr Research Activities are certified

- ISO 9001 V2015 (Quality),
- ISO 14001 V2015 (Environment),
- OHSAS 18001 (Health & Security).

Embedded systems at Thales

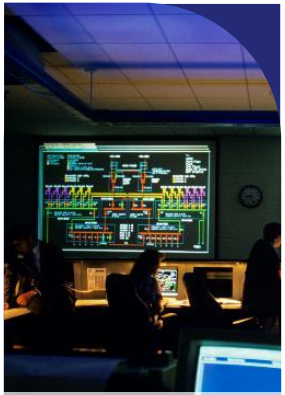
DUAL MARKETS
Military & Civil


AEROSPACE


SPACE


GROUND TRANSPORTATION


DEFENCE


SECURITY

Embedded computers are everywhere

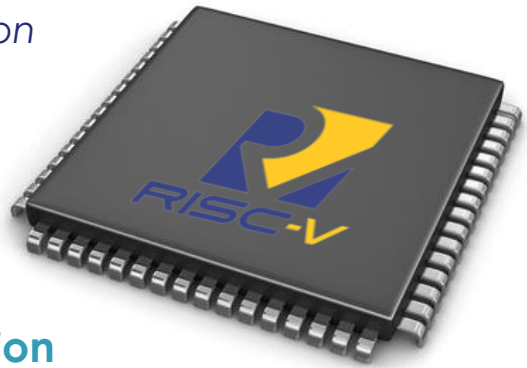
Why Thales invests in RISC-V (and open-source HW)?

Share cost instead of purchasing IP
Open-source community

Security
A fully auditable processor

■ Differentiator
■ Enabler

Sovereignty
Possible commercial exploitation without export constraints
Enable strong EU investment



No vendor-locking
Business opportunities for support, customization…

Safety
No black-box

Software
Large ecosystem compatible across implementations

SWaP & customization
Exact fit between features and application needs

Performance
State-of-the-art processor

Our RISC-V communities

RISC-V International (“the Foundation”)

- Specifies the open **RISC-V instruction set**
  - ✓ Simple & modular
  - ✓ 32- or 64-bit
  - ✓ Custom extensions
  - ✓ Covers a wide range of needs, **from MCU to HPC**
- Currently specifying **upcoming optional extensions**
- Hosts several **special interest groups** (SIG)
- Does not deliver implementations

GROUP OPENHW™ PROVEN PROCESSOR IP

OpenHW Group

- **Not-for-profit corporation** steered by its members
- Goal: deliver **open-source IP for production SoCs**
  - ✓ RISC-V compatible cores
  - ✓ SoC IP blocks
  - ✓ Verification environment
  - ✓ Supporting SW and tools
- Permissive, open-source, export-friendly **license**

Thales was the first French industrial company to join RISC-V as Platinum member in 2018.
Thales co-founded the OpenHW Group in 2019.

Open-source is suited for industrial use

Possible exploitation in product when permissive licenses are used

- Freely use, modify, integrate in proprietary solutions
- No need to publish modifications, no viral effect

Value generation

- Share cost instead of purchasing proprietary IP
- Customize for own application
- Increase control on your solutions
- Easier white box certification

Business models

- Commercial SW/HW/tooling add-ons
- Maintenance and support offers

Reduced supplier / export risks

- Ability to fork; no end-of-life
- Significantly lower exposition to export control

OpenHW governance

- Not-profit organization steered by its members
- Based on Eclipse Foundation's processes
- Target industrial-grade quality

Participation is encouraged

- Share IP development costs
- Influence technical content
- Get recognized as a contributor

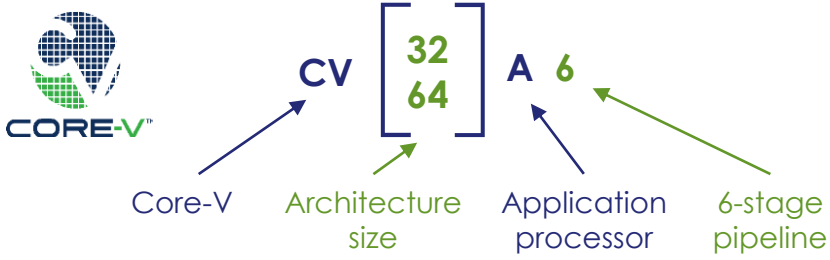
CVA6 core

Open-source RISC-V application core

- Supports rich OSes like Linux

Common source code, two flavors:

- CV64A6
  - 64-bit
  - ARIANE donated by ETH Zürich to OpenHW
- CV32A6
  - 32-bit
  - Compact version designed by Thales



An academic project turning into an industrial-grade CPU core

Réf. : TRT-Fr/STI/LCHP/NV,23/0027 – 29/09/2023
Thales Research & Technology France
Template trtp version 8,0,4 / template : 87211168-GRP-EN-005

{OPEN}

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CVA6 architecture

- Fully compatible with the RISC-V open ISA
- 6-stage pipeline, single issue, branch prediction
- L1 data and instruction caches
- AXI4 interfaces
- M/S/U privileges
- Safe and secure features
- MMU and memory protection
- Ready for multi/many-core CPUs
  - e.g. open-source OpenPiton framework

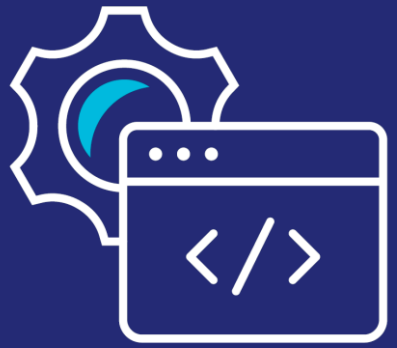
A 6-stage application CPU

Different cores, one solution

- 32/64 bit
- MMU / baremetal
- Floating-point: none, SP or DP
- Optional PMP (physical memory protection)
- Optional H (hypervisor) privilege mode
- Configurable L1 caches
  - Write-through/write-back
  - Size and number of ways
- Optional coprocessor interface (CV-X-IF)
- Design optimizations
  - ASIC/FPGA

Other options

- C, A, Zb* extensions
- Generic performance counters
- Bit extension on AXI (failure protection…)



Configure CVA6 for your application and constraints, either on ASIC and FPGA

All configurations are RISC-V compatible and supported by GCC compiler

An extendable core

CV-X-IF interface to extend the CVA6 instruction set

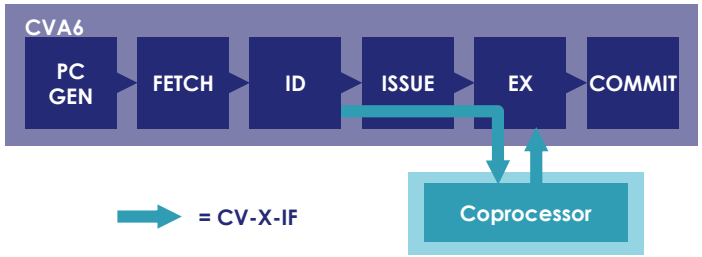
- Current or future RISC-V extensions (B, P…)
- Custom extensions (crypto, DSP, AI…)

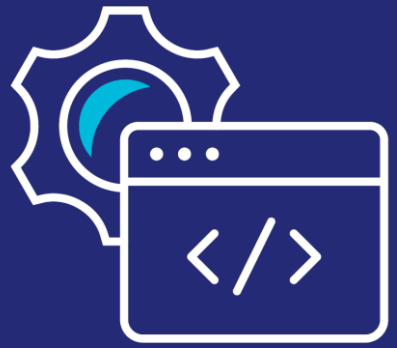
CV-X-IF specified by OpenHW Group

- Open specification, can be used off OpenHW
- Reuse coprocessors between CORE-V cores (CVA6, CV32E40X, CVE2)

Compiler support

- Seamless for RISC-V standard extensions (e.g. B)
- LLVM should ease the support of custom extensions
- Inline ASM possible for specific processing





Speed up your application with a custom accelerator

Add extensions without fully re-validating the core

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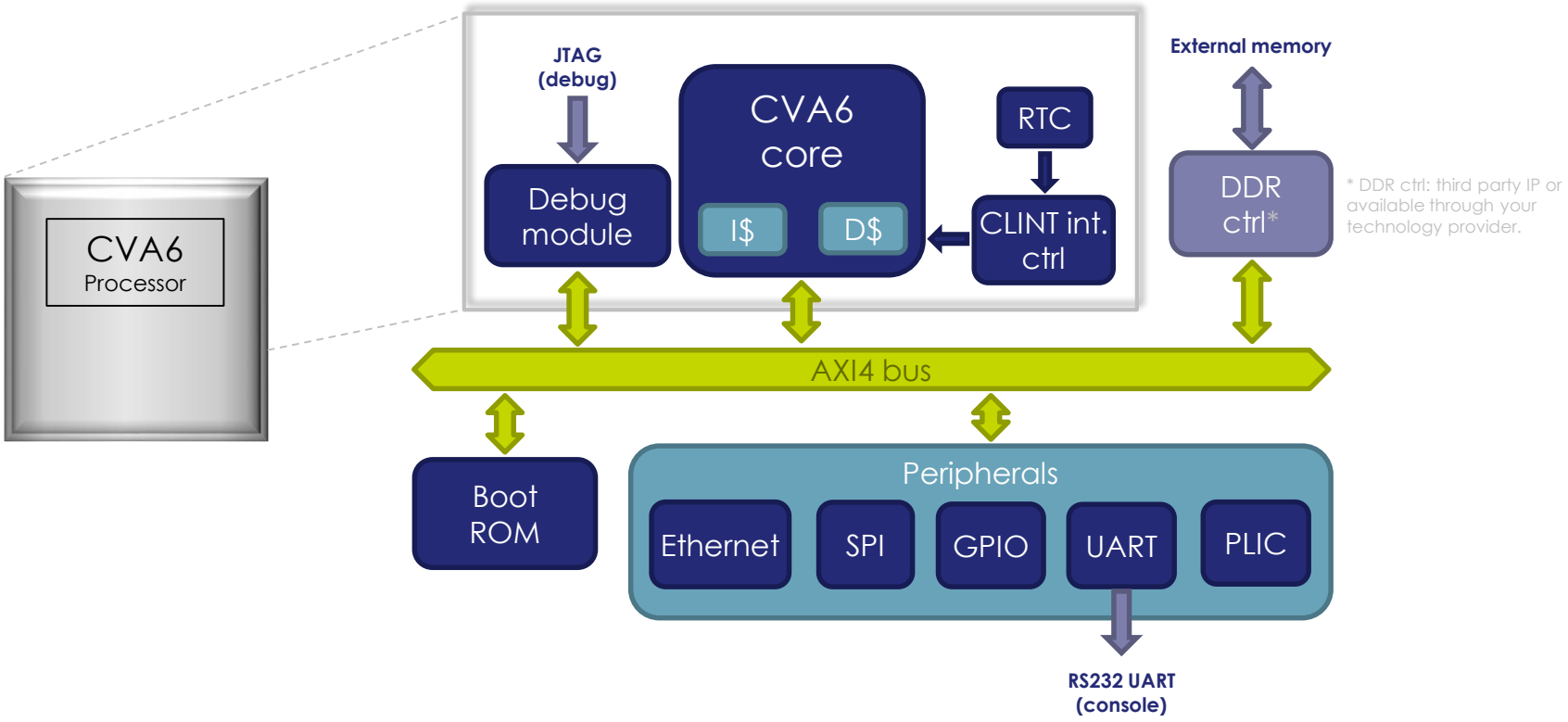
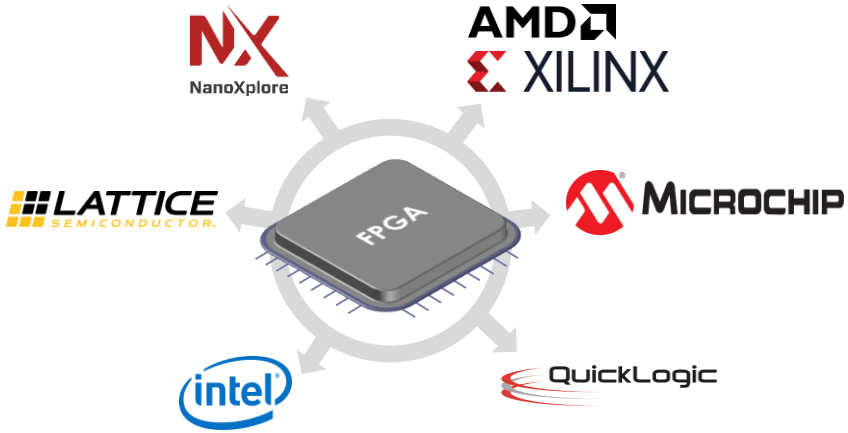
CPU sub-system



Multi-sourcing

- For **ASIC targets** (32/64 bit)
- For **any FPGAs** (32 bit)

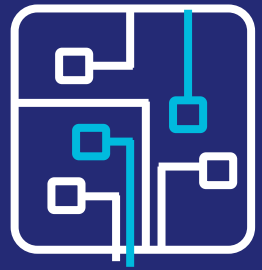


Leverage your investment: reuse your HW/SW architectures throughout your product range (multi-sourcing: any ASIC and FPGA vendors)

HW implementations

CV32A6	FPGA			
Frequency	189 MHz			
Performance	2.8 CoreMark/MHz 530 CoreMark			
Resources	8,108 LUT	4,534 FF	12 BRAM	4 DSP
Technology	Zynq UltraScale+ -3			
Configuration	RV32IMA, 8K D$ + 8K I$, noFPU, MMU			

CV32A6	ASIC
Frequency	900 MHz
Performance	3.09 CoreMark/MHz 2781 CoreMark
Resources	80 kgates
Technology	28 nm (worst case corner)
Configuration	RV32IMA, 8K I$ + no D$, noFPU, MMU



Ongoing work.

More optimizations are coming!

SW ecosystem

OPENHW GROUP — PROVEN PROCESSOR IP

Boot and FW

- **U-Boot**
- **OpenSBI**

U-Boot · yocto PROJECT · freeRTOS

OS support

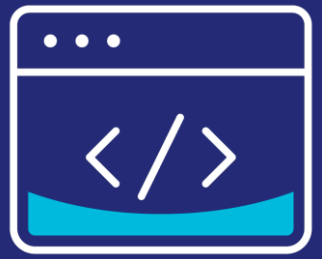
- **Linux:** 32 & 64 bit
- **Yocto** honister, Buildroot 2021.08
- **FreeRTOS:** 32 & 64 bit
- **RTEMS** 6
- CVA6 compatible with many others

Compiler

- Standard **GCC** (11.2, 13.1)
- Libraries: **glibc** (2.70), Newlib 4.3.0…
- CLANG/LLVM 16, **RUST**

Debug

- HW and baremetal: JTAG probe, OpenOCD, GDB 13
- Linux-based: GDB server, GDB/Eclipse IDE



Full open-source software ecosystem

Protect your HW investments

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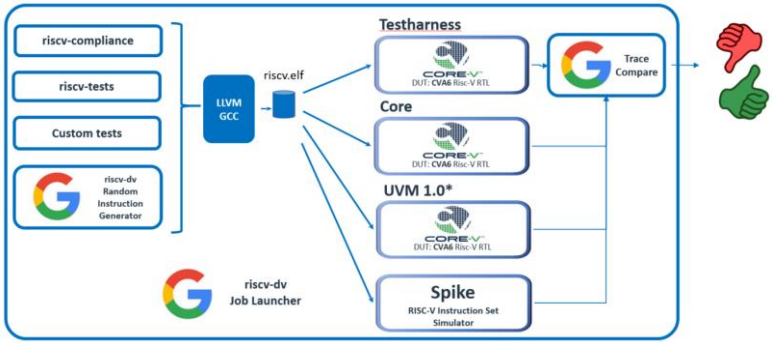
CVA6 verification

Continuous integration (CI)

Leverages Google open-source components and OpenHW methodology

Next steps:

- Complete UVM testbench
- New test sequences
- 100% functional coverage (UVM-based)



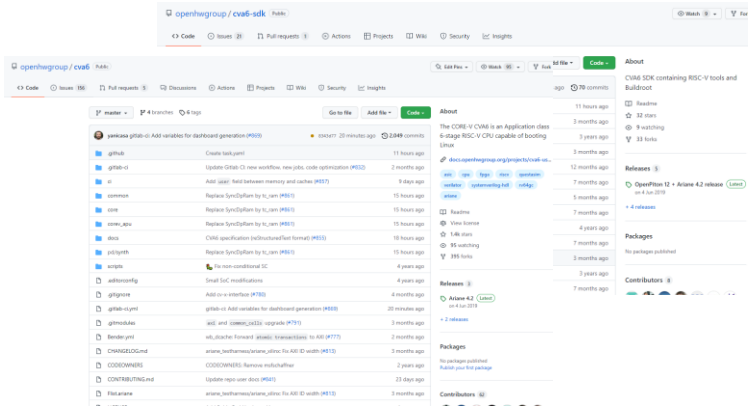
Verification artifacts will be available as open-source.

Target is 100% verification coverage.

Open-source project

Complete open-source package

- CVA6 core
- Verification: testbench, sequences, ISS…
- Linux, FreeRTOS support
- SolderPad HW license (no contamination)



https://github.com/openhwgroup/cva6
https://github.com/openhwgroup/cva6-sdk
https://github.com/openhwgroup/meta-cva6-yocto

Evaluate CVA6 now for your next products generation

Open-source eases collaboration.

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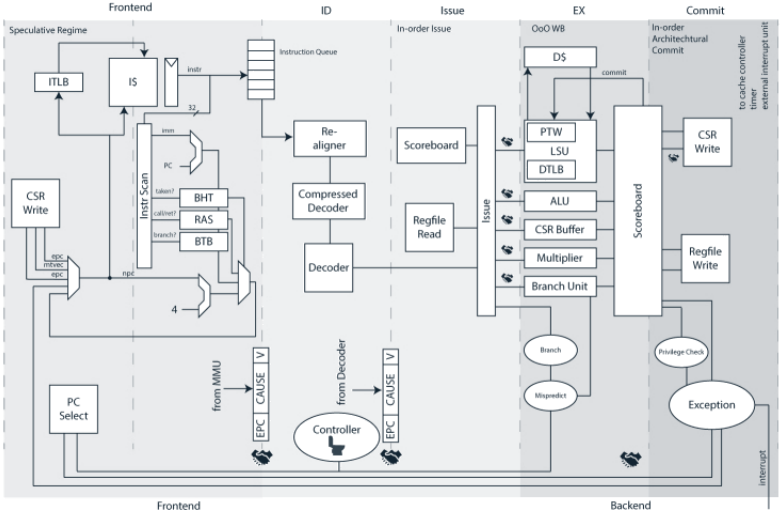
Thales contributions: design of a 32-bit CVA6

Results

Mainly supported by Thales DIS/INVIA.

- Functional 32-bit version of the CVA6
  - 32-bit MMU for Linux (TRT)
  - New caches, register sizes and RF (Thales DIS)



CV32A6: RV32IMA[F][C]_Zicsr_Zifencei M/S/U [Sv32]

CV64A6 - RV64IMA[F[D]][C]_Zicsr_Zifencei M/S/U[/H] [Sv39]

Thales contributions: FPGA optimizations

Results:

- Frequency improvement: +40% maximal frequency (⇗ **140MHz**).
- Resources reduction: **-55%** of LUTs, **-61%** of FFs and -75% of BRAMs.
- Same CoreMark as the Xilinx proprietary Microblaze.
- The CV32A6 soft-core is becoming competitive in terms of PPA on Xilinx FPGAs.

What is coming next?

- Optimizations for Microchip PolarFire and Intel Stratix FPGAs.
- All optimizations will be made available soon in open-source (https://github.com/openhwgroup/cva6).

This TRT activity is supported by:

The **FRACTAL** project is funded under H2020 ECSEL GA n°877056

Thales contributions: Linux Yocto on CVA6 & debug

Up-to-date Yocto embedded Linux released:

- The most popular distribution generator for embedded systems
  - Linux kernel 5.10.7.
- 32- and 64-bit support
- Built upon **U-Boot** and **OpenSBI**

This TRT activity is supported by:

The **FRACTAL** project is funded under H2020 ECSEL GA n°877056

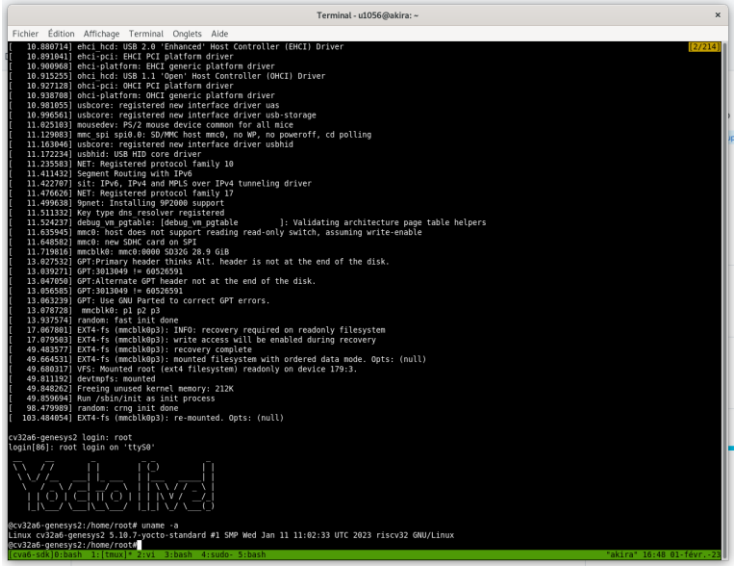
The **TRISTAN** project is funded under Horizon Europe KDT GA n°101095947

Debug environment

- Demo with debug toolchain (with Eclipse).

Available here:

https://github.com/openhwgroup/meta-cva6-yocto
https://github.com/openhwgroup/cva6-sdk



Demo'22: Linux running on the CV32A6 softcore

Demonstrates maturity

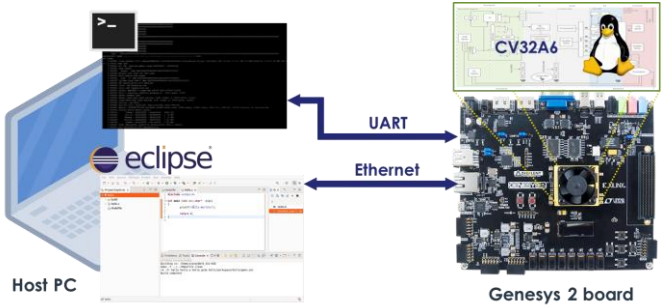
- Implementation on the Genesys-2 FPGA board*
  - Kintex7 (XC7K325T-2FFG900C)
  - DDR3
  - Programmable over JTAG and Quad-SPI Flash
  - Ethernet Link with the host
- State-of-the-art boot flow
  - U-Boot
  - OpenSBI
  - Buildroot 2021.08
- Linux OS running

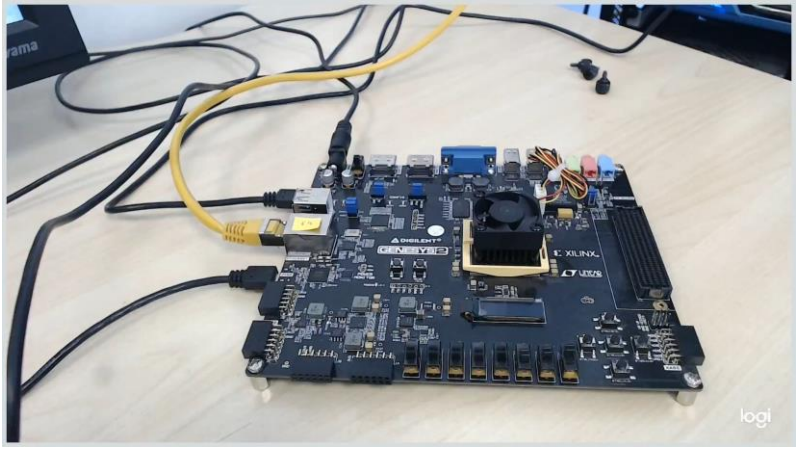
U-Boot

OpenSBI

Ready for SW development

- GNU/Linux standard developer tools
- Eclipse IDE debug environment





Fully open source stack from software to hardware

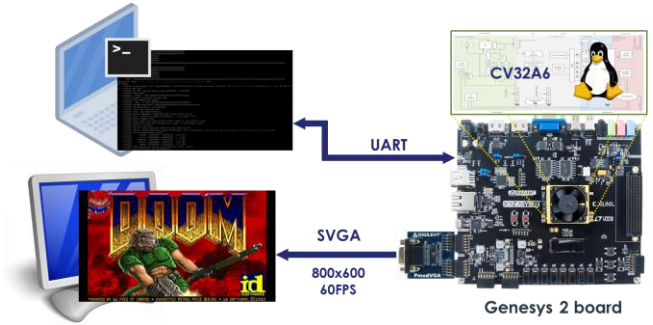
*Also works on Microsemi Polarfire

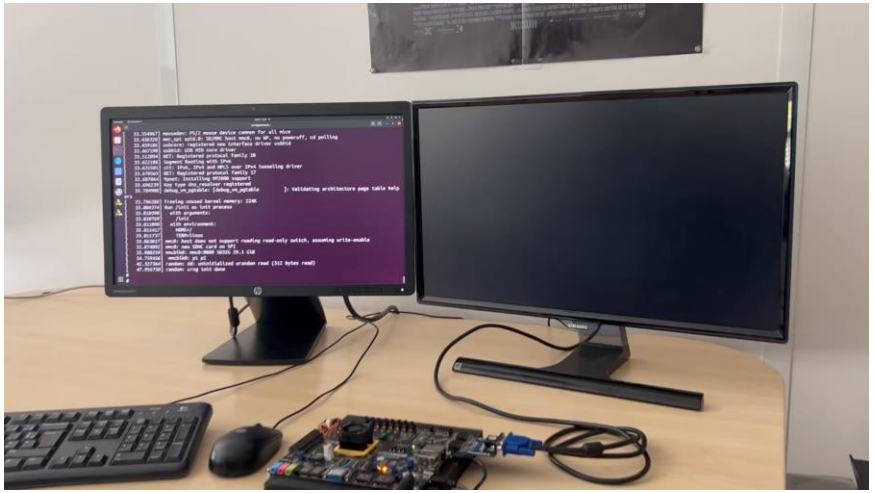
Demo'23: Doom on the CV32A6 soft-core

Demonstrates performance

- Support of high-level software applications
- Implementation on the Genesys-2 FPGA board
  - Kintex 7 (XC7K325T-2FFG900C)
  - DDR3
  - PMOD-VGA connected to a monitor
- Yocto Linux OS
- VGA framebuffer integration
  - SVGA 800x600 at 60FPS
- Chocolate-doom
  - 15 FPS

Ready for Thales products
(e.g. augmented reality, embedded HMI)





Thales contributions: safety & security

Secure V (ANR)

- Context-dependent monitoring, run-time probes
- Dynamic memory management
- CFI use-case

Execution at RISC: Stealth JOP Attacks on RISC-V Applications

- L. Buckwell, O. Gilles, D. Gracia Pérez, N. Kosmatov
- https://arxiv.org/abs/2307.12648

Upcoming:

- Detection of execution flow anomalies in real-time embedded systems (PhD)
- Formal verification: ramping up on CVA6
- Safe multi-core
- Safety island

OpenHW Group & projects

OpenHW Group

- Non-profit, steered by its members
- Organized as tasks groups and projects
- Primary focus on production-grade IP (TRL5)
- Great home for research (TRL3)

OpenHW Group
PROVEN PROCESSOR IP

OpenHW Group French members

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cea
SCIENCES SORBONNE UNIVERSITÉ
GREENWAVES TECHNOLOGIES
KALRAY

Project phases

PC: Project Concept	*Why should OpenHW do this project? Who's in?*
PL: Project Launch	*How is the project organized? What are the main deliverables?*
PA: Plan Approved	*Feature list / specification Project plan*
Project work	
PF: Project Freeze	*RTL Freeze checklist or other checklist*

Open-source hardware boosts innovation, impact, influence & recognition

RISC-V student contest

Organized by

Objectives

- Promote RISC-V and computer architecture in French education
- Extend RISC-V and OpenHW communities
- Strengthen industry-academy connections

Past editions

- 2020-2021: Improve CV32A6 FPGA performance
  - 13 teams from 10 universities
  - Awarded: Télécom Paris, U. Toulouse III
- 2021-2022: Improve CV32A6 energy efficiency
  - 12 teams from 7 universities
  - Awarded: U. Strasbourg (2 teams), IMT Atlantique
- 2022-2023: Focus on CV32A6 cybersecurity
  - 19 teams from 14 universities
  - Awarded: INSA Toulouse, CentraleSupélec

RISC-V student contest: what's coming?

2023-2024: Accelerating AI applications on CV32A6

- Modify CV32A6 architecture to accelerate a CNN recognizing MNIST digits
- Skills: Digital electronics, HDL, simulation, computing architecture, embedded programming, AI acceleration, FPGA
- Teams up to 4 master students presented by French academies
- Prizes: 5000 € + 3000 €
- Timeline:
  - Good fit for academic projects
  - November 2023: technical kit available
  - May 13th, 2024: deadline to submit results
- Contacts and registration:

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pascal.benoit@lirmm.fr

Conclusion

Development of an industrial-grade open-source processor

- TRT is focusing on the CV32A6 soft-core optimized for FPGAs and its Linux support

A fast growing HW/SW ecosystem around CVA6

- New industrials are joining the initiative, as well as new academics labs

A good sandbox to ease collaborative work between academics and industrials

- And working together will prevent fragmentation

"Technology is best when it brings people together"
Matt Mullenweg

Acknowledgements

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Thank you.

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