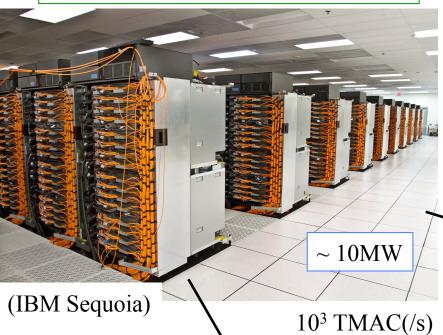
Ultra-Low Power Embedded IoT Machine Learning enabled through FPAAs

Professor Jennifer Hasler Georgia Institute of Technology http://hasler.ece.gatech.edu



Embedded Machine Learning

Machine Classification and Learning: What we currently think

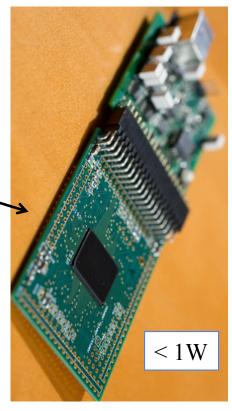


Powered

by

Machine Classification and Learning: What we want

Presentation begins to build this transformation



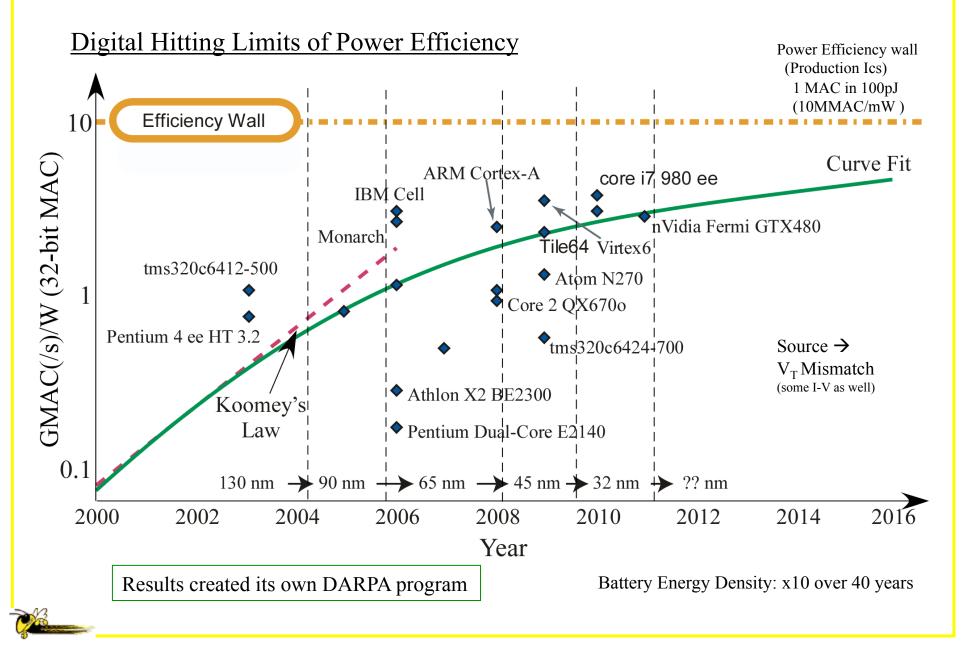
10 TMAC(/s)

Physical Computing > Increased Computational Efficiency

Large-Scale Field Programmable Analog Arrays (FPAA) x100016k x 16 **Improvement SRAM** x1000Physical Computation Improvement **CMOS** Scaling 10MMAC(/s)/W10MMAC(/s)/mW (1979)Energy (2010)10MMAC(/s)/mWEfficiency Wall Wearable Devices Require more Efficiency

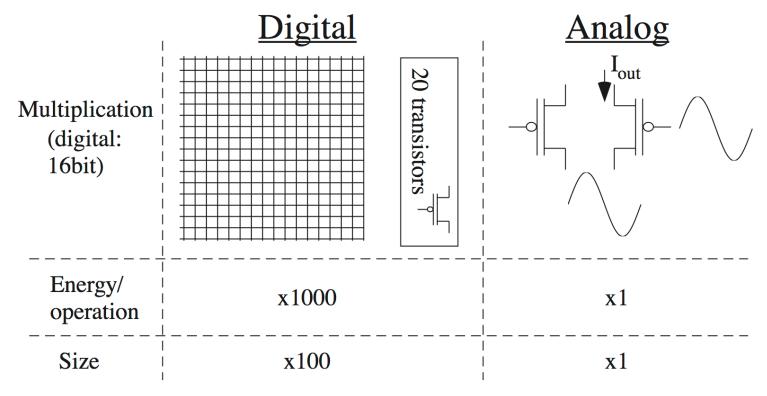


Why Analog (Physical Based) Processing?



Why Analog (Physical Based) Processing?

Mead Hypothesis (1990): Analog x1000 efficiency improvement



• Analog (VMM): ~100 fJ / MAC (10MMAC/μW) @ yield

• Other Analog SP similar: Freq Decomp / Analog FT

VMM, GMM

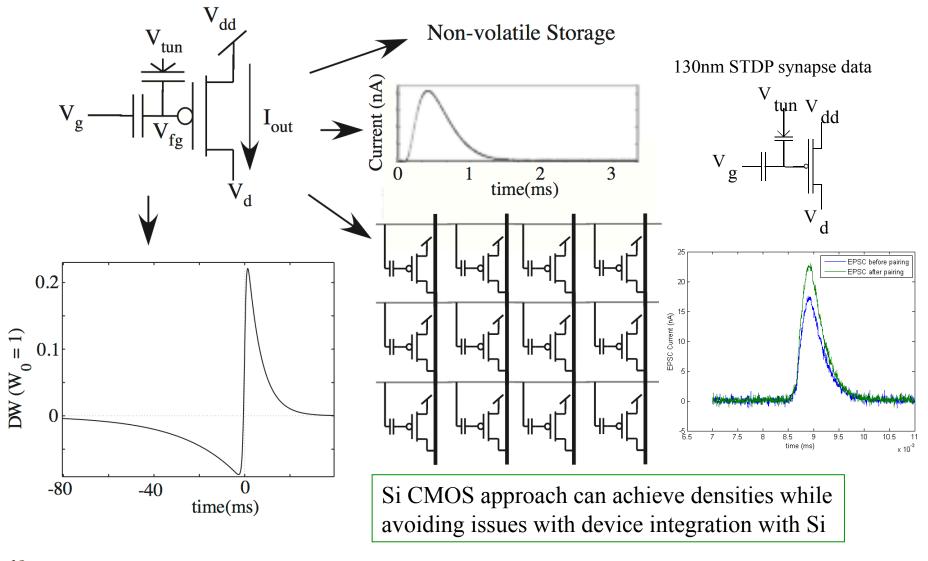
Classifiers

Adaptive Filters



Single-Transistor Learning Synapse

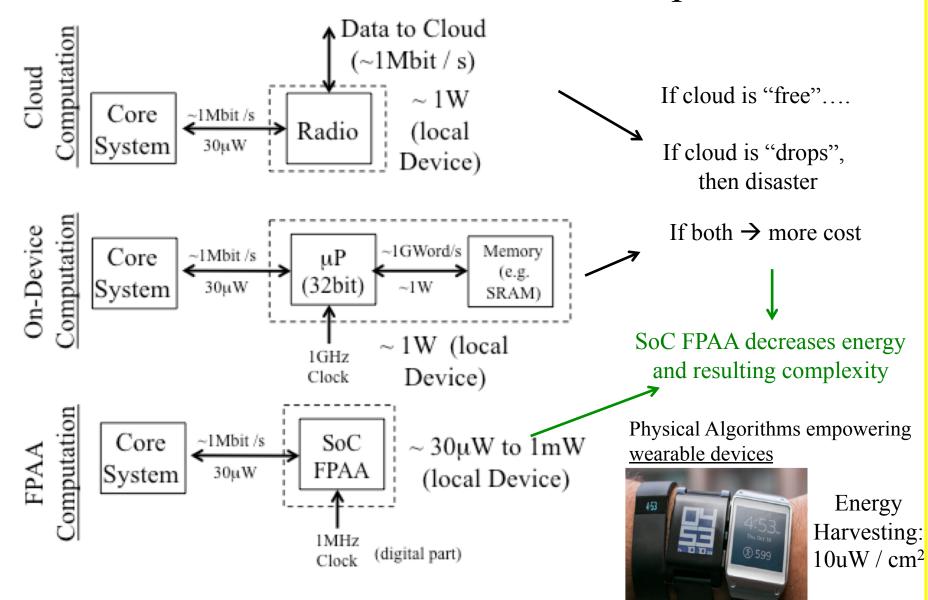
Floating-Gate Circuits: Nonvolilative storage, computation, programmable, adaptable





[Hasler, et. al, NIPS 1994, BMES 1994, and later papers]

FPAA vs. Embedded / Cloud Computation





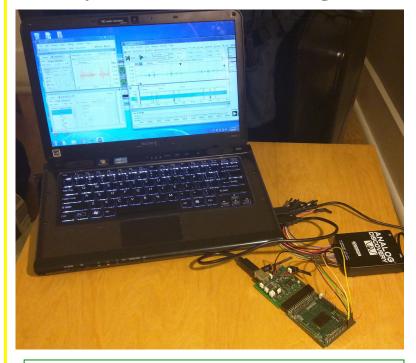
Where to use ultra-low energy?

Sensor node $\leq 100 \mu W$

x1000 energy improvement utilizes context-aware physical computing to enable 100µW end-to-end sensor node.

Sensor_ Inputs	Stage 1	Stage 2	Stage 3	Stage 4
	Continuous	Classification	Second Wakeup	Full Processing
	Operation (analog)	(analog + digital)	(e.g. processor wakeup)	(e.g. Transceiver)
Average on time	100%	1-3%	0.1-0.2%	0.01%
Operating power	1 to 10μW	~100µW	1-5mW	30-100mW
Total(max) Power	10μW	$3\mu W$	$10\mu W$	10μW
Digital		<1MMAC/s	~10-20MMAC/s or 20MHz clock	Transciever on
Analog	10-100MMAC/s	1GMAC/s	50GMAC/s	
More computation				
Increasing Energy Decreasing Use				

Physical / Analog / Mixed-Signal Computing Exists





imaging
On-chip Machine

sensors, acoustics,

Analog + Digital

Applications in

FPAA

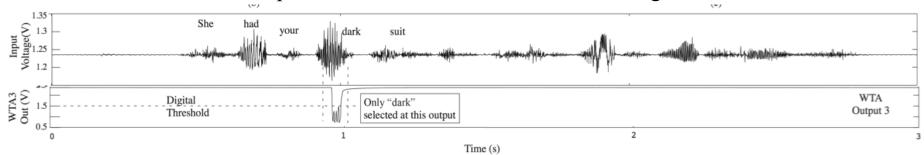
On-chip Machine learning shown (VMM+WTA)

Command Word < 23µW power

Knee-Joint Rehab $\leq 15 \mu W$

Capability over multiple IC processes

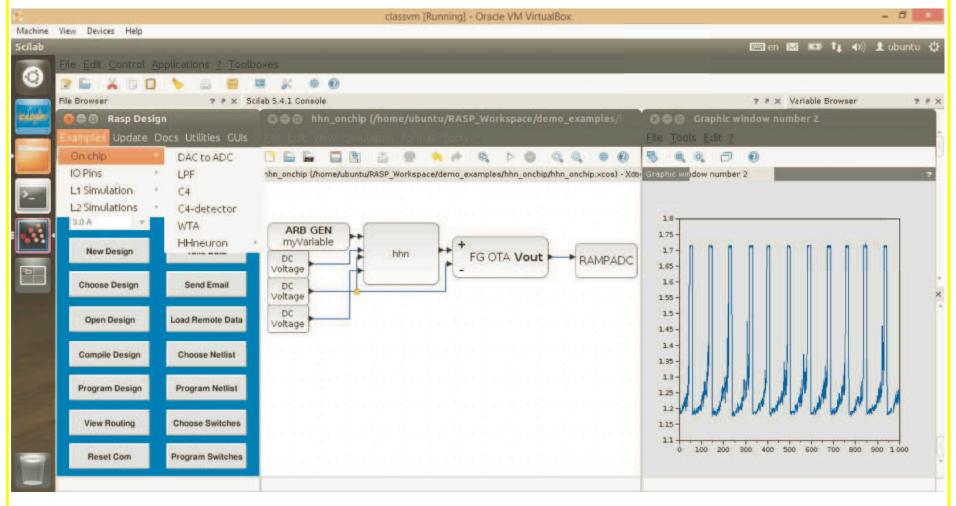
Measured Results for a phrase from the TIMIT database to recognize the word "Dark"





RASP 3.0: First SoC FPAA IC FPAA Fabric Array Input Lines $|\mathbf{D}||\mathbf{D}$ D A |D||DΑ D Α **SRAM** Program: 16k x 16 D D D D D Α A A D A CLB Data: 16k x 16 D JTAG: 8n1 D D D D D serial port MSP430 Α D D Α Open Core Processor D D Α D **BLE** D $|\mathbf{D}|$ D D D Α Α D D D Α D Α D 16bit GP input D D D D Α Α D $||\mathbf{A}||$ Memory $\|\mathbf{D}\|$ D D Α D $|\mathbf{D}||\mathbf{A}$ **Output Lines** Mapped 16bit Registers $|\mathbf{D}||\mathbf{D}$ Input Lines D A Α D $|\mathbf{D}||\mathbf{A}$ GP output GND D Α D Α D CAB/ 3 SPI GP I/O CLB D Α D D Α Α D $|\mathbf{D}||\mathbf{A}|$ CAB **Ports** D SPI D D Α D A D $\mathbf{D} || \mathbf{A}$ Prog: I→ V Computational Analog and/or **Ports** Ramp ADC D' D D D D D Α A Α Α digital Block **CAB CAB** CLB N W S E N'W'S'E S Block: CAB **CAB CLB** Routing to Routing x2CAB / CLB Lines $1M\Omega$ GND GND x^2 $100k\Omega$ C Block: Routing Lines **Routing x4** to CABs **GND GND** 10kΩ <u>x4</u> 0 0.5 1.5 **Output Lines** $V_{s}(V)$

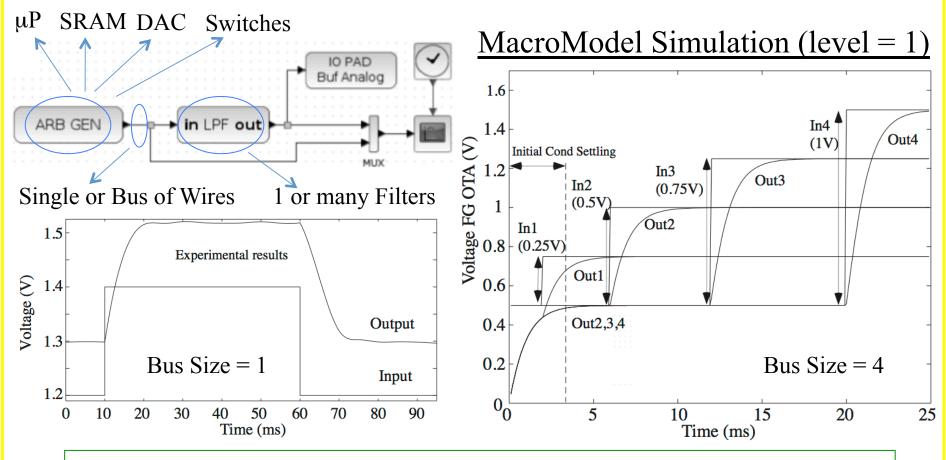
Scilab FPAA Synthesis & Modeling Tool



- Encapsulated in Ubuntu 12.04 VM
- Library of Components (low to high level)
- Measurement transistor channel model of HH neuron



Tool: Measurement and Simulation (LPF)



One toolset to design, to enable high level simulation, and to compile to hardware

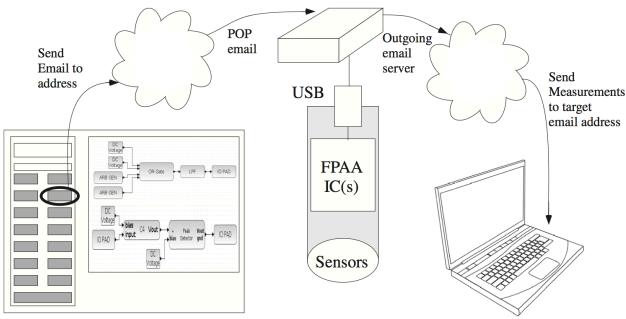




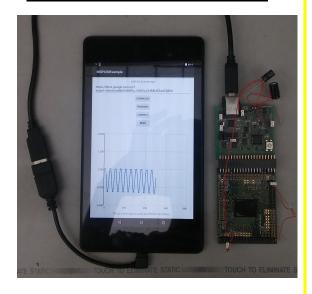
Remote FPAA System

FPAA Infrastructure

- FG Programming looks like controlled download to μP device → Straightforward to program a device (code in Scilab, Python, Java,)
- USB powered and controlled → interfaces like a digital system

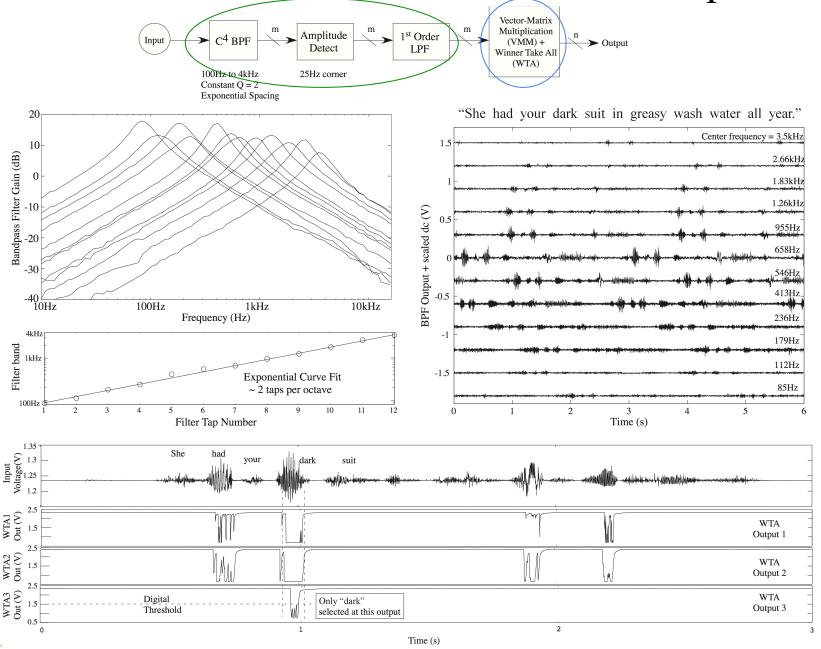


Andriod Tablet FPAAs



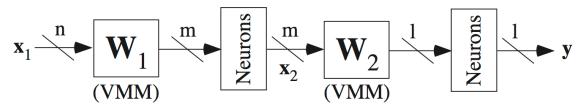


SoC FPAA Classifiers: VMM + WTA for Speech



Compiled VMM+WTA Classifier

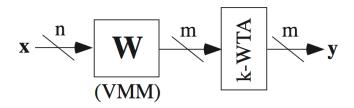
Two-Layer Neural Network (NN) Classifier



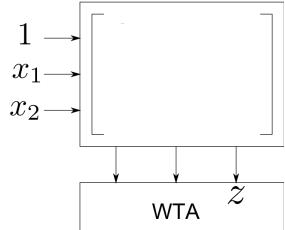
Minsksy 1967: XOR classification requires more than one layer

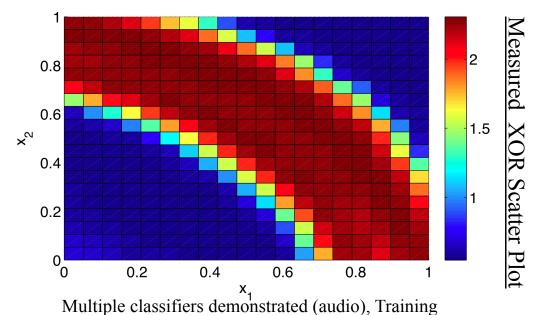
NN was silenced for 15 years Could solve in **two** layers

VMM+WTA Classifier



3 x 3 VMM



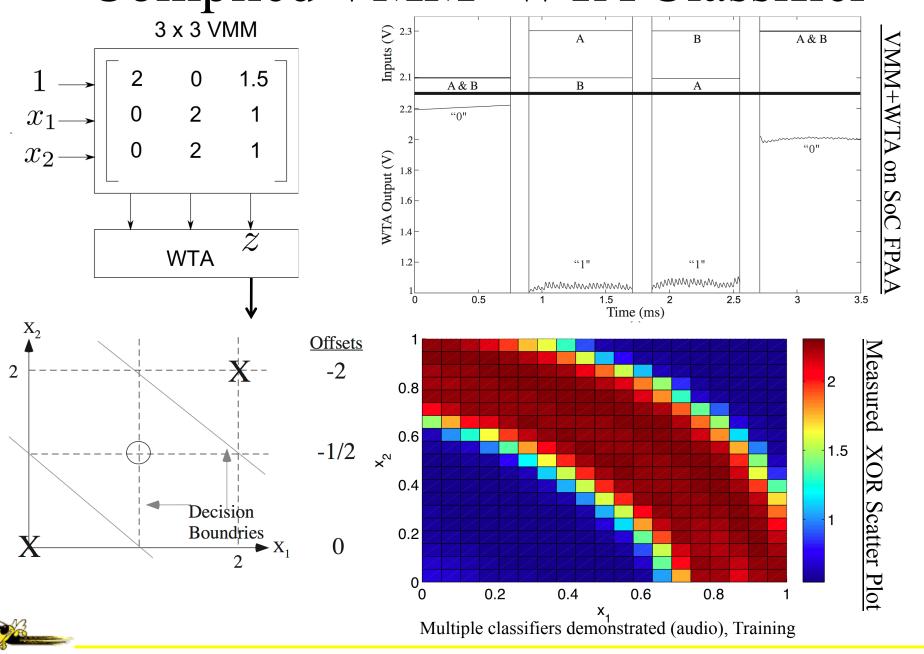


Analog, n-WTA single layer block can be a universal approximator (2 layer NN)

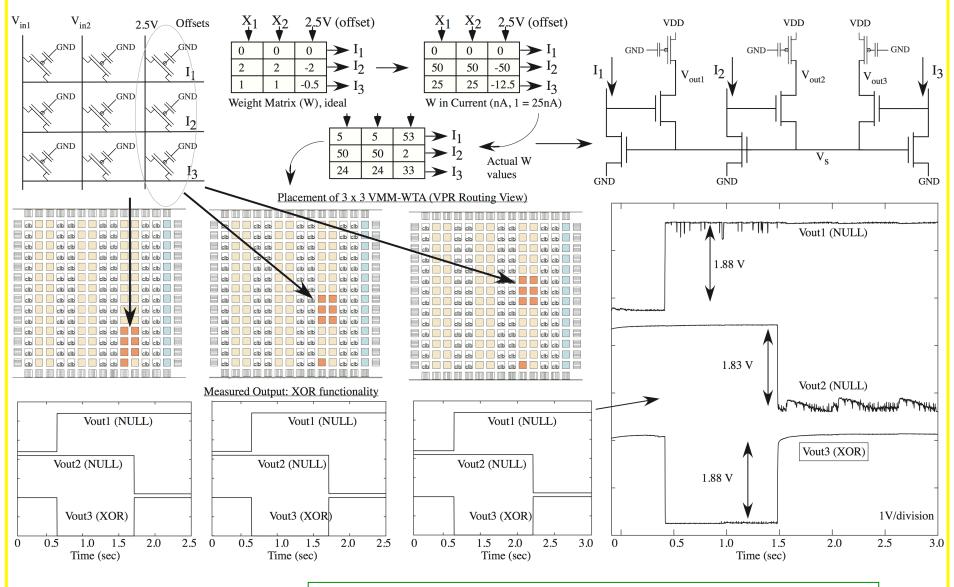
[Maass, et. al, 2000, Ramakrishnan, et. al, 2013]



Compiled VMM+WTA Classifier

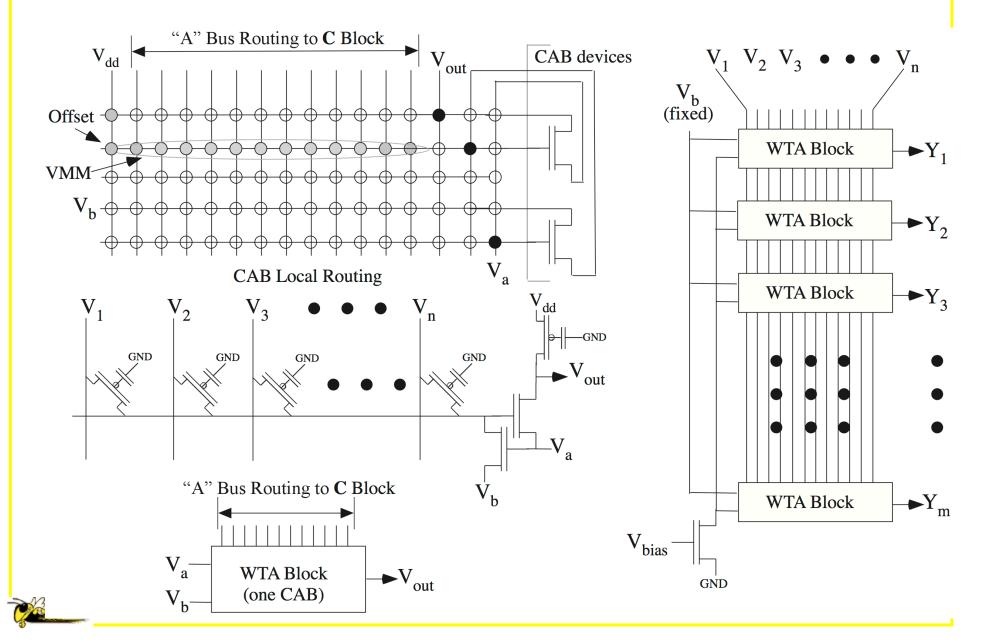


Measured XOR Classifier: Different CABs

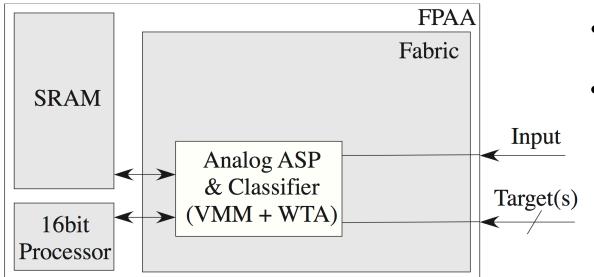




Physical FPAA Classifier Floorplan

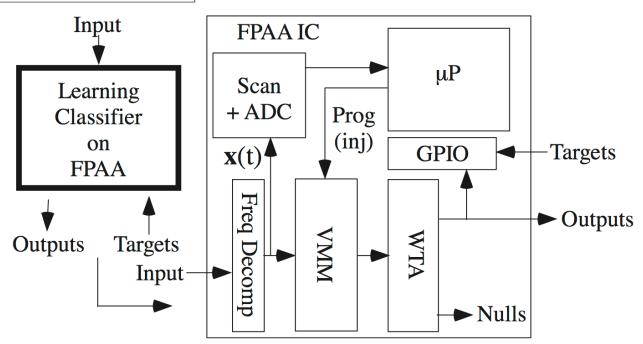


Developing FPAA Adaptation



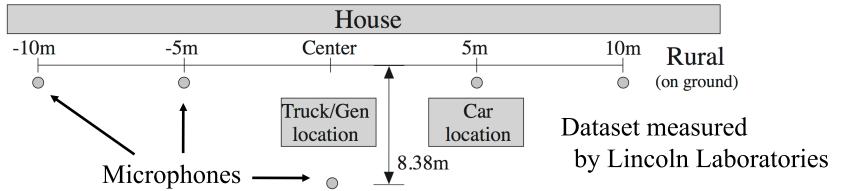
- Analog, Digital, and μP
- FG Programming uses μP device (Batch)
- Analog classifier, ultralow energy datapath

- Microphone input to classification
- statistics: analog or digital
- infrastructure and ADCs

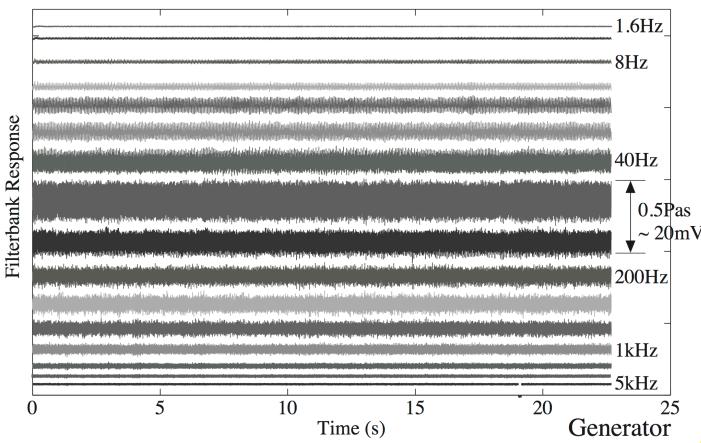




Acoustic Classification Training Data



• Two minutes sensor recording (simultaneous)

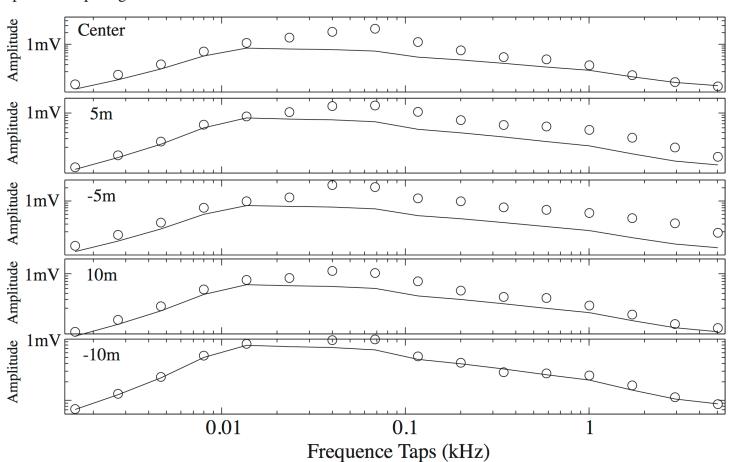




Acoustic Classification >> FPAA

FPAA Datapath **Vector-Matrix** <u>Architecture</u> Multiplication Amplitude 1st Order C⁴ BPF Input (VMM) +Detect LPF Winner Take All (WTA) < 5Hz corner < 5Hz corner 8Hz to 4kHz Constant Q = 2**Exponential Spacing**

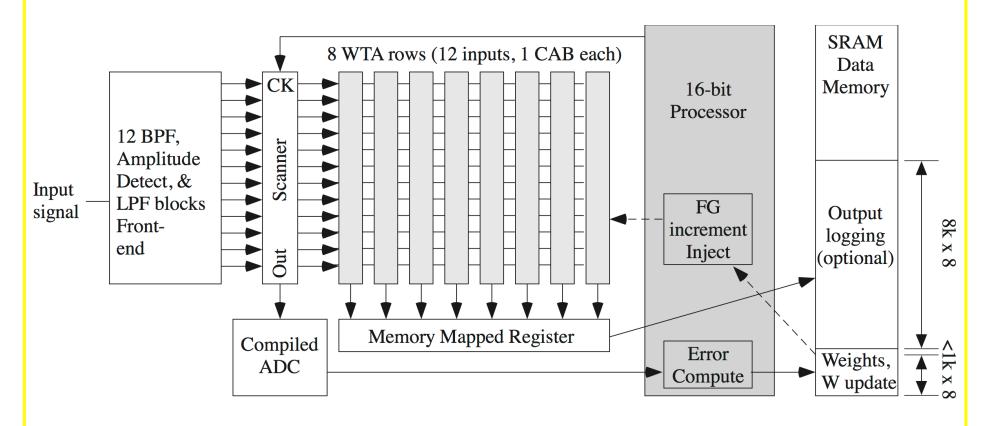
- Amplitude vs. frequency for different distances
- Somewhat
 robust
 frequency
 features
 & complex
 background
 noise



➤ Output



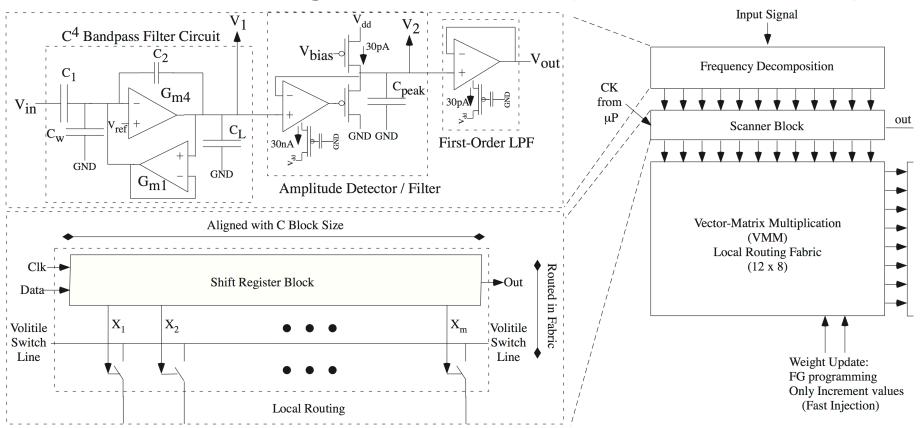
Developing FPAA Adaptation



- Combined Analog, Digital, and μP Architectural Design
- FG Programming uses μP device (Batch)
- Analog classifier, ultra-low energy classifier datapath



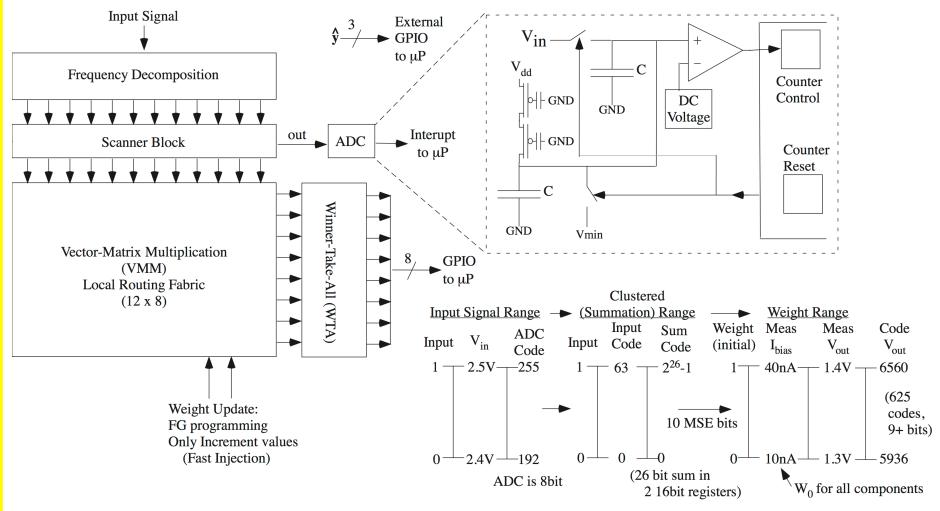
More Analog Classifier (VMM+WTA)



- Front-End Circuit blocks, "scanning" blocks to enable training
- VMM implemented in local-fabric routing



More Analog Classifier (VMM+WTA)



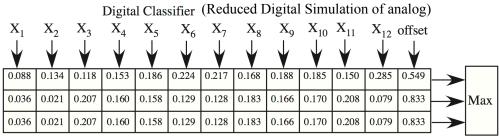
- Error metrics and FG update programming handled through μP
- Requires careful scaling of fixed-point arithmatic



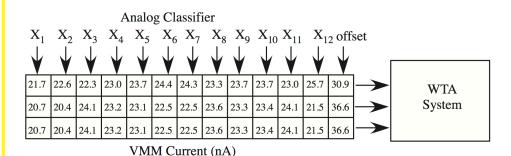
Analog Learning Classifier (VMM+WTA)



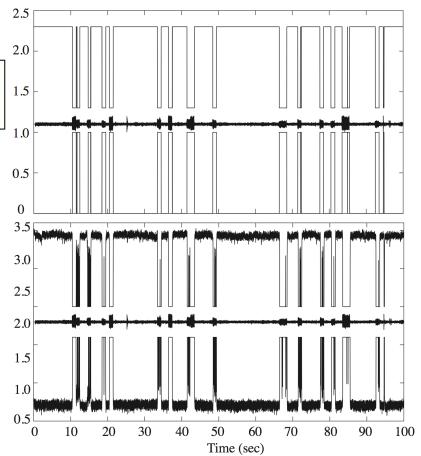
Detect one acoustic signal (1s signal bursts)



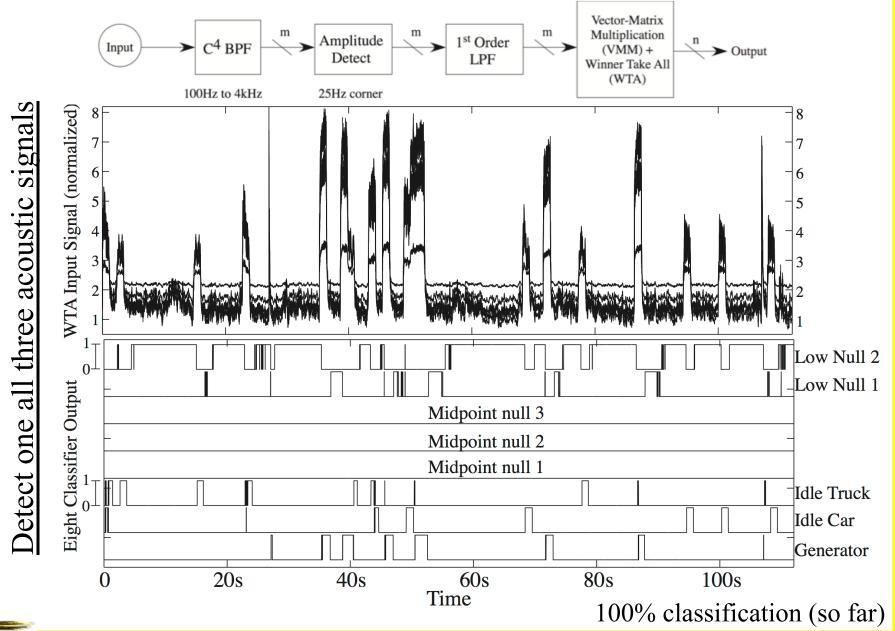
Digital Weights



100% classification (so far)



Analog Learning Classifier (VMM+WTA)



Neuromorphic + Analog Computation

