GDR SoC^2 Workshop on

"Functional Safety of SoCs and AI Hardware"

Tuesday, April 28th, 2020

Sorbonne Université, Campus Jussieu, LIP6, 4 place Jussieu, 75005 Paris, room 25-26/105

Organizers:

Haralampos-G. Stratigopoulos, Sorbonne Université, CNRS, LIP6, Paris

Patricia Desgreys, TELECOM Paris, Paris – Palaiseau

Scope:

Integrated circuits and electronics are ubiquitous in today's world with numerous and ever-expanding applications. Several of these applications are considered to be safety-critical and/or mission-critical, i.e., electrical vehicles, autonomous vehicles, smart healthcare, defense, critical infrastructure, etc. In this case, electronics demand functional safety features. Functional safety refers to the requirement to equip chips with automatic protection during normal operation. This includes correct operation in response to all inputs even under non-intended use or sometimes even misuse, detection of reliability hazards, prevention of failures that could be detrimental, detection of failures when they occur, and controlling failures when they occur ideally recovering from them using fault-tolerance, self-repair, or self-healing principles. Meeting functional safety standards first of all necessitates robust designs with proven reliability. Then, thorough post-manufacturing testing is required to screen out faulty devices and outliers. During the application, self-test and on-line test are required to detect failures and an error tolerance and/or error recovery strategy needs to be devised to ensure uninterrupted operation. On-chip sensors and reliability monitors play a key role in self-test mechanisms and error recovery feedback loops.

This workshop aims at discussing trends and cutting edge approaches for functional safety of general Systems-on-Chip (SoCs), as well as for Artificial Intelligence (AI) hardware which is

an emerging class of SoCs. Nowadays, there are intense efforts in designing specialized AI hardware that are motivated by two objectives, namely AI hardware accelerators and AI edge computing. As AI hardware will play a central role in near future safety-critical applications, such as remote-controlled sensor networks and autonomous vehicles, guaranteeing its functional safety will be one of the key technology enablers.

The areas of interest related to SoCs and AI hardware include (but are not limited to):

- Reliability analysis and design-for-reliability
- On-chip automated and secure test infrastructures
- On-chip sensors and reliability monitors
- Built-in self-test and design-for-test
- On-line test
- Fault-tolerance, self-healing, and self-repair
- Fault diagnosis and on-line diagnostics
- Pre-silicon verification and post-silicon validation

This workshop traverses two axis of GDR SoC^2, namely:

- Axe "Frontières et interfaces cyberphysiques"
- Axe "Sécurité et intégrité des systèmes"

Preliminary Program:

Prof. Georges Gielen, KULeuven, Belgium, will give a keynote titled:

"Towards Unfailing Analog Circuits for Biomedical and Automotive Applications"

This keynote is sponsored by the IEEE Circuits and Systems (CAS) Society under its Distinguished Lecturer Program (DLP).

Submissions:

If you wish to give a talk please submit a title and abstract by sending an e-mail to Haralampos at haralampos.stratigopoulos@lip6.fr by Tuesday, March 31st, 2020. Notifications will be sent out by Friday, April 3rd, 2020.

Registration:

The workshop participation, including coffee breaks, lunch, etc., is free of any charge. To help the organizers with the logistics please register by sending an e-mail to Haralampos at haralampos.stratigopoulos@lip6.fr by Monday, April 6th, 2020.