PHD Thesis Proposal
Low-Power IOT System Architectures

Description

One of the major trends in the IoT field is to move computation tasks from distant location (cloud) closer to the sensor location (edge computing). These computations usually involves both Deep Neural Network utilization and traditional signal processing algorithms to perform first treatment and/or classification from sensor data prior to a RF (BLE, 5G, …) transmission. The goal is to shorten the system response time and lower the power enabling a longer battery lifetime by reducing the amount of data exchanged through the highly consuming RF link. To meet these challenges, the approach requires to design circuits with both high computation power and energy efficiency.

The objective of this PhD thesis is to setup computation engine with extremely low power consumption optimized for a target applications. The first targets will be audio processing algorithm (keyword spotting, Natural Language Understanding, beamforming, noise cancellation, …) Depending on the progress and result obtained, the work will be extended to other application domains like image recognition, data processing from sensors, …

The study of the algorithm and its evaluation will enable to define an energy efficient architectures mixing software running on processors with hardware accelerators and optimized memory access management.

The indicative list of tasks to complete during the thesis is as follow:
- Perform bibliography analysis of the State of the Art
- Analyze and evaluate NN algorithm for a target application
- Develop High level modeling of the data treatment chain
- Define, evaluate and setup the target software/hardware architecture
- Contribute to the specifications of analog IPs (power management, Audio, memories) optimized for their usage into the architecture
- Define, setup and treatment of measurements performed on the demonstration circuit exploiting the solution developed during PhD (~1 chip / year)
- Write technical papers and present it into conferences

This thesis will be co-directed by Dolphin Integration and the AMfoRS research group of the TIMA laboratory (a joint research laboratory led by CNRS, Grenoble INP and Université Grenoble-Alpes). The thesis will be carried on mainly at Dolphin Integration, one of the main leaders of Low-Power mixed signal IPs and platform. AMfoRS group in TIMA Laboratory targets crucial challenges regarding the reliability and security of low power hardware architectures dedicated to embedded AI applications.

Starting Date: September 1st 2019

Contract type: Permanent position
Target Salary: 32k€
Main technical skills required during this PhD:
- Embedded Software/Algorithm : C / C++ / ASM
- RTL design: verilog/system Verilog, C/C++ for HLS (High Level Synthesis)
- System modeling : SystemC / Matlab Simulink/Python

ELIGIBILITY CRITERIA

Applicants must hold a Master's degree (or be about to earn one) or have a university degree equivalent to a European Master's (5-year duration).

Applicants will have to send an application letter in English and attach:

- Their last diploma and transcript of last 2 years scores.
- Their CV focusing on the technical topics developed and implemented in projects and labs
- A short presentation of their scientific project (2 to 3 pages max)
- Letters of recommendation (at least one)

Contact:
alena.gili-tos@dolphin.fr
Lorena.anghel@grenoble-inp.fr