Stage de Master - Master thesis

Title: Impact analysis of micro-architecture modifications for transient computing

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Context:

The raise of the ubiquitous computing leads to the design of connected and communicating object spread out in our environment. The main challenge in designing these objects is then to reduce their energy consumption. One emerging solution proposed to address part of this problem is the normally-off computing paradigm. Normally-off computing is made possible thanks to the advent of new non-volatile memory (NVM) technologies based on spintronics, and on the design of Non-Volatile µ-processors.

NVM technologies are now sufficiently advanced for components to be commercialized, and even integrated in off-the-shelf ultra low-power SoCs alongside a conventional memory hierarchy, like the TI MSP429 ultra low-power platform integrating a Ferroelectric RAM (FRAM) module alongside a small SRAM. Questions are open concerning more complex integration scheme in the architecture of SoCs and works are still carried on.

Objective:

In the NOPE project (collaboration with IRISA, LS2N and IETR labs) we will focus on normally-off computing for small embedded systems. These systems are typically built using an ultra low-power System-on-Chip (SoC) and an embedded operating system (OS) tailored for their specific needs (limited memory and processing power, limited memory hierarchy, no hardware support for virtual memory, real-time scheduling). In this domain, pushing further energy efficiency enables to envision transiently powered systems that work without any battery, using energy harvested from the environment.

This internship position intends to study the main challenging points of designing a Non-Volatile Processor that will support efficiently dedicated services of the OS for transient computing. The read and write latencies achieved by today’s NVM technologies are now small enough to consider to include them at different levels of the memory hierarchy: main memory, cache, or even register files for micro-controllers. Non-volatility enables normally-off behavior, while implementing such memories at L1 or register level enables instant-on. In this study we will study different technologies of NVM and evaluate their ability to be implemented and used at different level of the memory hierarchy of a processor. Additionally the power constraints will be considered in this work.

References